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WEATHER SATELLITE PICTURE RECEIVING STATIONS, APT DIGITAL SCAN CONVERTER

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16. Abstract The Automatic Picture Transmission (APT) Digital Scan Converter is used at APT ground stations to convert signals received from APT scanning radiometers to data compatible with ground equipment designed to receive signals from APT vidicons aboard operational meteorological satellites. All information necessary to understand the circuit theory, functional operation, general construction and calibration of the converter is contained in this document. Brief and detailed descriptions of each of the individual circuits are contained herein. Each is accompanied by a schematic diagram contained at the end of each circuit description. Additionally, listings of integral parts and testing equipment required as well as an overall wiring diagram are included. This unit, which can be constructed from locally procured, low-cost components, when connected between the RF receiver and the output display unit at the ground station, will enable the user to readily accept and process, as required, weather photographs from the operational meteorological satellites.					
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This document makes use of international metric units according to the Systeme International d'Unites (SI). In certain cases, utility requires the retention of other systems of units in addition to the SI units. The conventional units stated in parentheses following the computed SI equivalents are the basis of the measurements and calculations reported.

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WEATHER SATELLITE PICTURE RECEIVING STATIONS, APT DIGITAL SCAN CONVERTER

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INTRODUCTION

Automatic picture transmission (APT), a direct readout of weather photographs from operational meteorological satellites, is presently used by over 100 countries as a basic part of their forecast service. Some of the electro mechanical display equipment at the receiving stations are not readily adjustable to the format of the new APT scanning radiometers that has replaced the old APT systems used over the past 10 years. In addition to the different scanning rate, the APT system does not correct for the panoramic distortion inherent in scanning the curvature of the earth's surface. In many display equipments, the data received from the satellite may be shown directly with no modification. Most frequently, the electro mechanical displays found in the receiving stations are not easily converted to accept data of a time-based difference and/or to perform the selection and correction of the APT data necessary for meaningful picture processing. It is for these reasons that the APT Digital Scan Converter was developed.

The converter is connected between the RF receiver and the input to the hard copy/visual display in the receiving system of the APT ground station. It electronically alters the APT data received from the satellite.

Figure 1 is a photograph of the prototype of the APT Digital Scan Converter, built at NASA, which is an inexpensive and reliable solution to the data display problem. It can be built by anyone competent in digital electronics from off-the-shelf components which are readily available in most parts of the world.

The information necessary to understand the circuit theory, functional operation, and general construction of the converter is provided herein. Also provided are detailed circuit and wiring drawings, photographs and dimensional data which should be used as a guide to the mechanical construction of the unit. A unit built in another part of the world may differ with respect to personal preference and local component availability.

GENERAL DESCRIPTION

Physical

For portability and ease of construction, the APT Digital Scan Converter is housed in a standard electronics equipment case measuring 28 by 28 by 46 cm (11 by 11 by 18 in.); the



Figure 1. APT Digital Scan Converter

unit weighs approximately 9 kg (20 lb). Contained in the case is a 25 by 40 by 7.5 cm (10 by 17 by 3 in.) preformed chassis onto which are mounted nine circuit card holders, three power supplies, and the front panel of the unit. The power and some cabling connections are located on the rear of the chassis, with the remainder of the cabling connections and the operational controls located on the front panel.

Functional

The converter receives data synchronous with a 48-rpm scanning radiometer in a meteorological satellite. The converter demodulates a 2.4 kHz subcarrier, and processes the resulting video. The video is filtered and processed to reduce aliasing in the video in the digitized form. Additionally, the scan converter provides the option to correct for the earth's curvature, if so desired. After analog processing, the one scan line of video is digitized and stored in memory. At the first opportunity, the digital data is clocked out of memory at a rate compatible with the scanning rate of the display monitor and reconverted to an analog signal. This video is used to modulate a 2.4 kHz subcarrier which is filtered and provided to the display monitor. (See figure 2.)

Satellite Data Format

To understand the principle of operation of the converter, it is necessary to first understand the data format of the signal received from the satellite.

Figure 3 shows that IR and VIS data are transmitted alternately. The beginning of each transmission is marked by 7 cycles of 300 Hz which is followed by 24.45 ms of pre-earth scan. It is important to note that the voltage levels of pre-earth scan for IR is opposite to that of VIS. That is, pre-earth for IR is at a high voltage level and the voltage for VIS is low. These two parameters (the sync bursts and the pre-earth scan) enable a logic to be devised which allows the scan converter operator to select the data (VIS or IR) he wishes to examine.

Next in the sequence is 377.78 ms of earth scan data. This time is fixed by the angular velocity of the satellite's scanning radiometer (48 rpm) and the ratio of the satellite altitude and earth's diameter. Other data, not pertinent to this scan converter, are transmitted in the following 199.44 ms after which the alternate sequence begins.

SYSTEM AND CIRCUIT DESCRIPTIONS

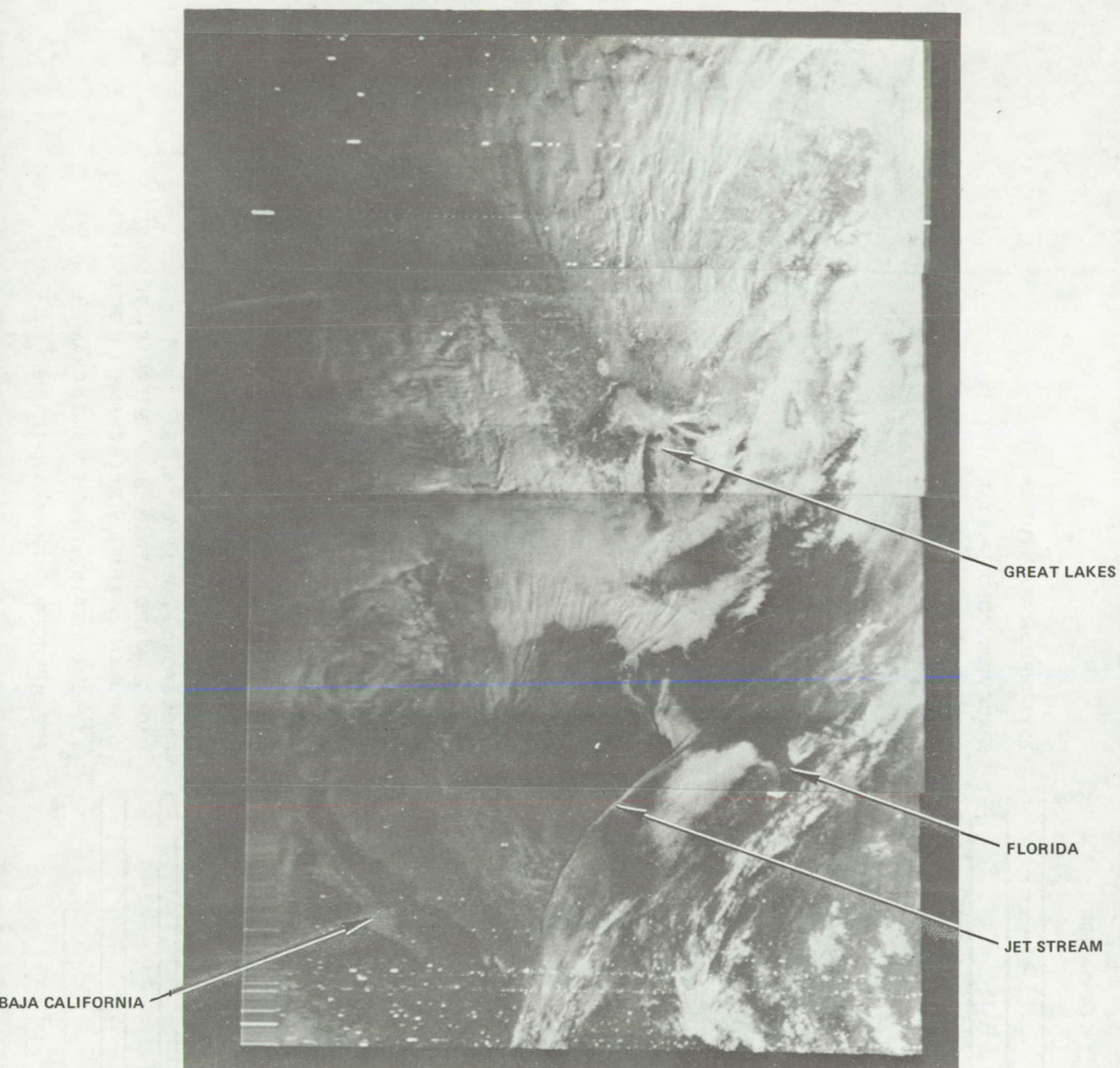
System Description

The APT Digital Scan Converter basically performs the following functions:

1. Detects the 300 Hz sync burst,
2. Performs IR/VIS selection by pre-earth examination,
3. Selects the portion of earth surface to be examined,

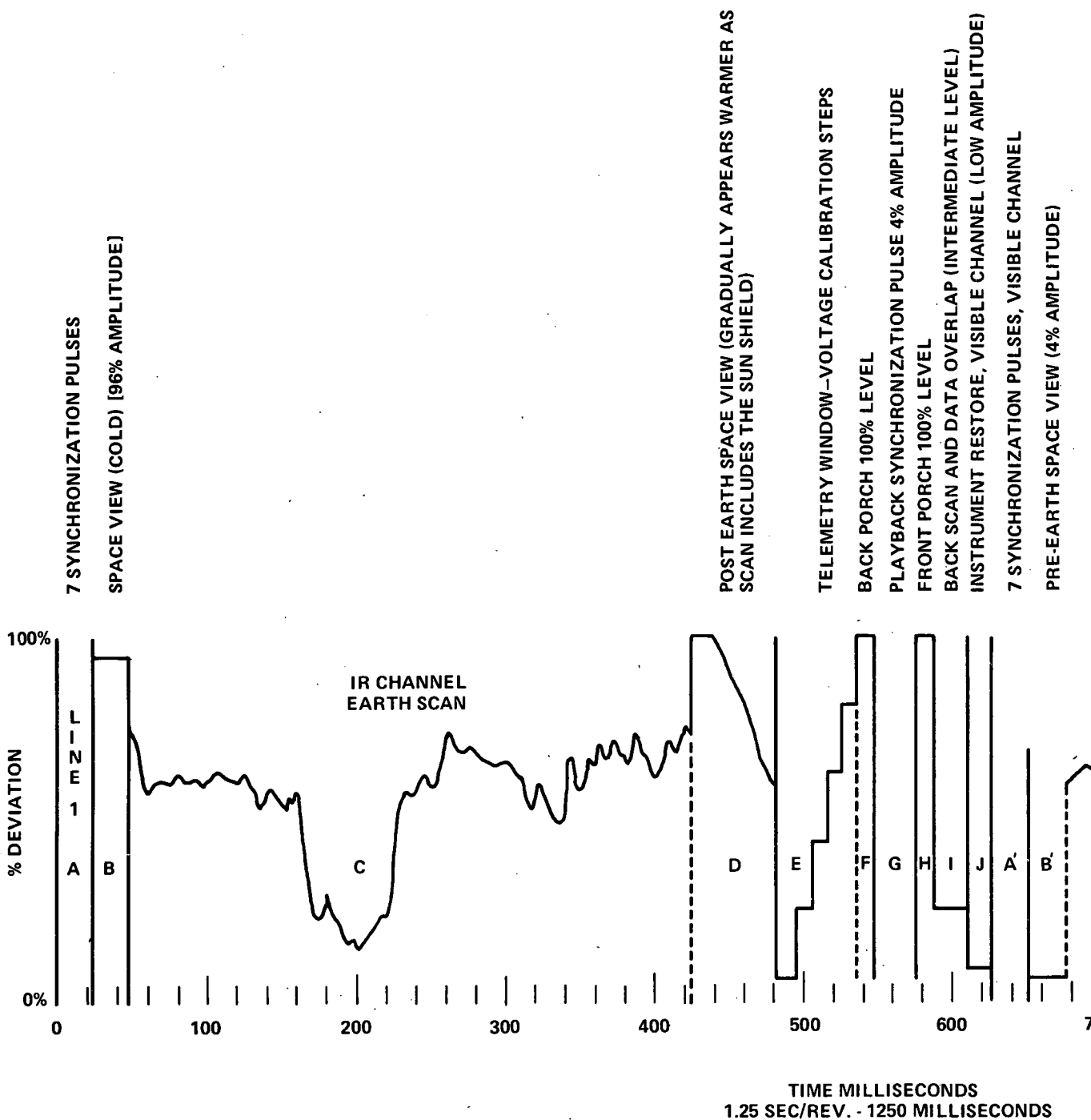


A. Normal Nonlinearized 48 RPM Presentation



B. 120 RPM Scan Converted Linearized Presentation

Figure 2. APT Facsimile Output (North America, Eastern Half)



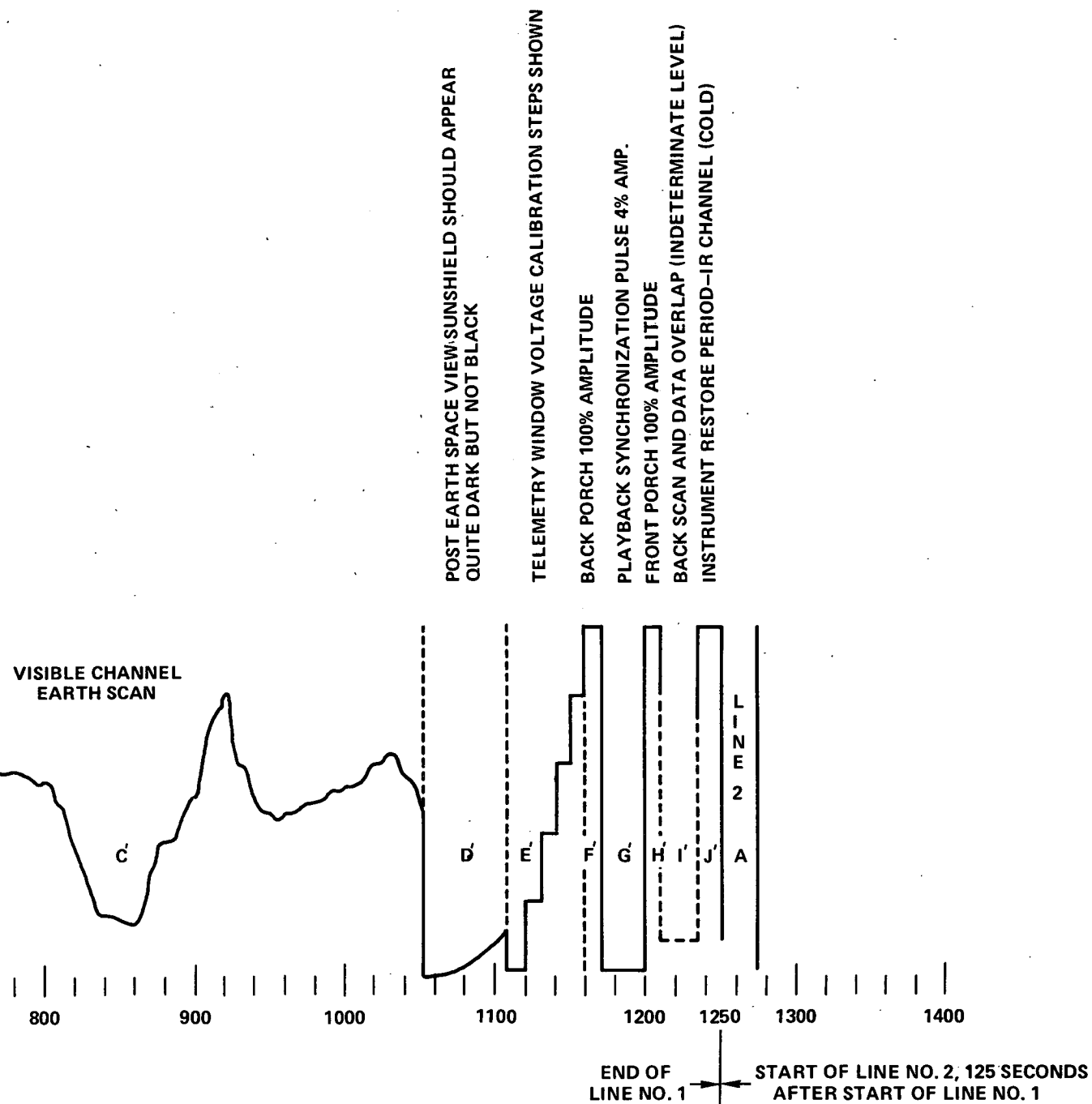


Figure 3. SR Sensor-APT-Signal Characteristics

4. Reformats the data in a time base compatible with the time base of the display, and
5. Corrects for panoramic distortion, if desired by the scan converter operator.

The 2.4 kHz amplitude modulated data enters both the Sync Pulse Generator Card (Card 6) and the Analog Signal Processing Card (Card 4) simultaneously (figure 4).

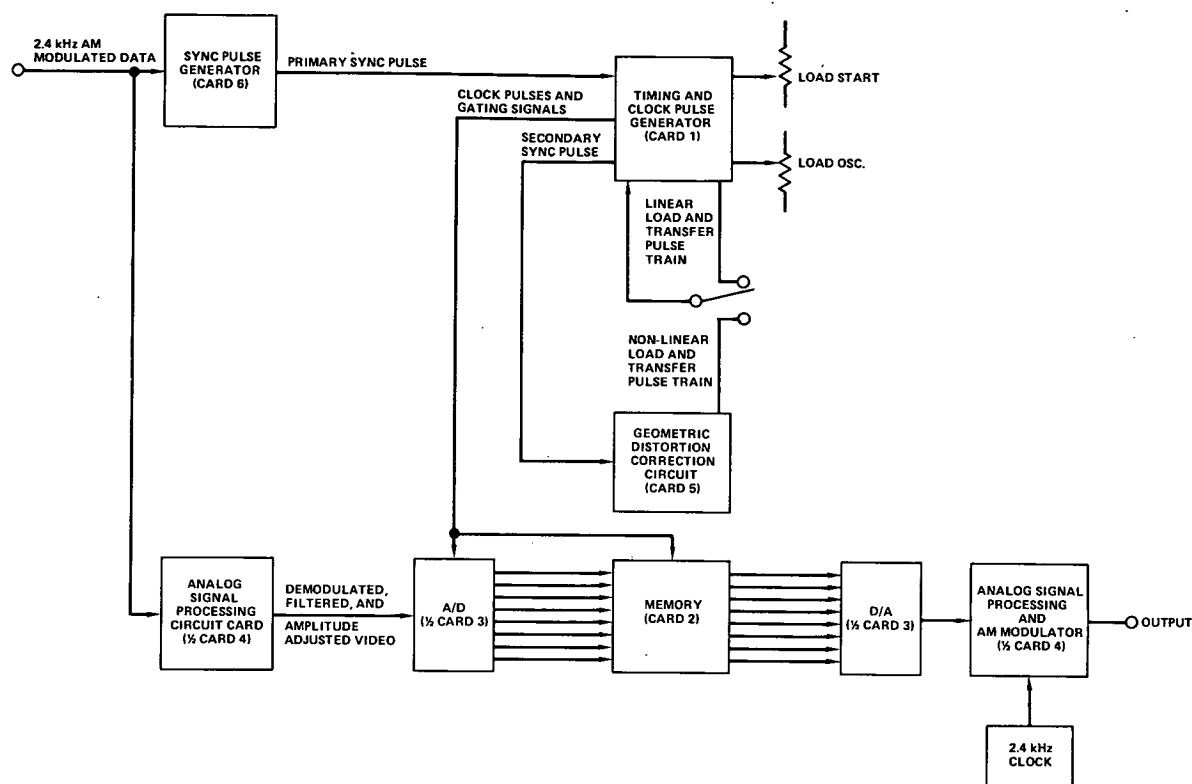
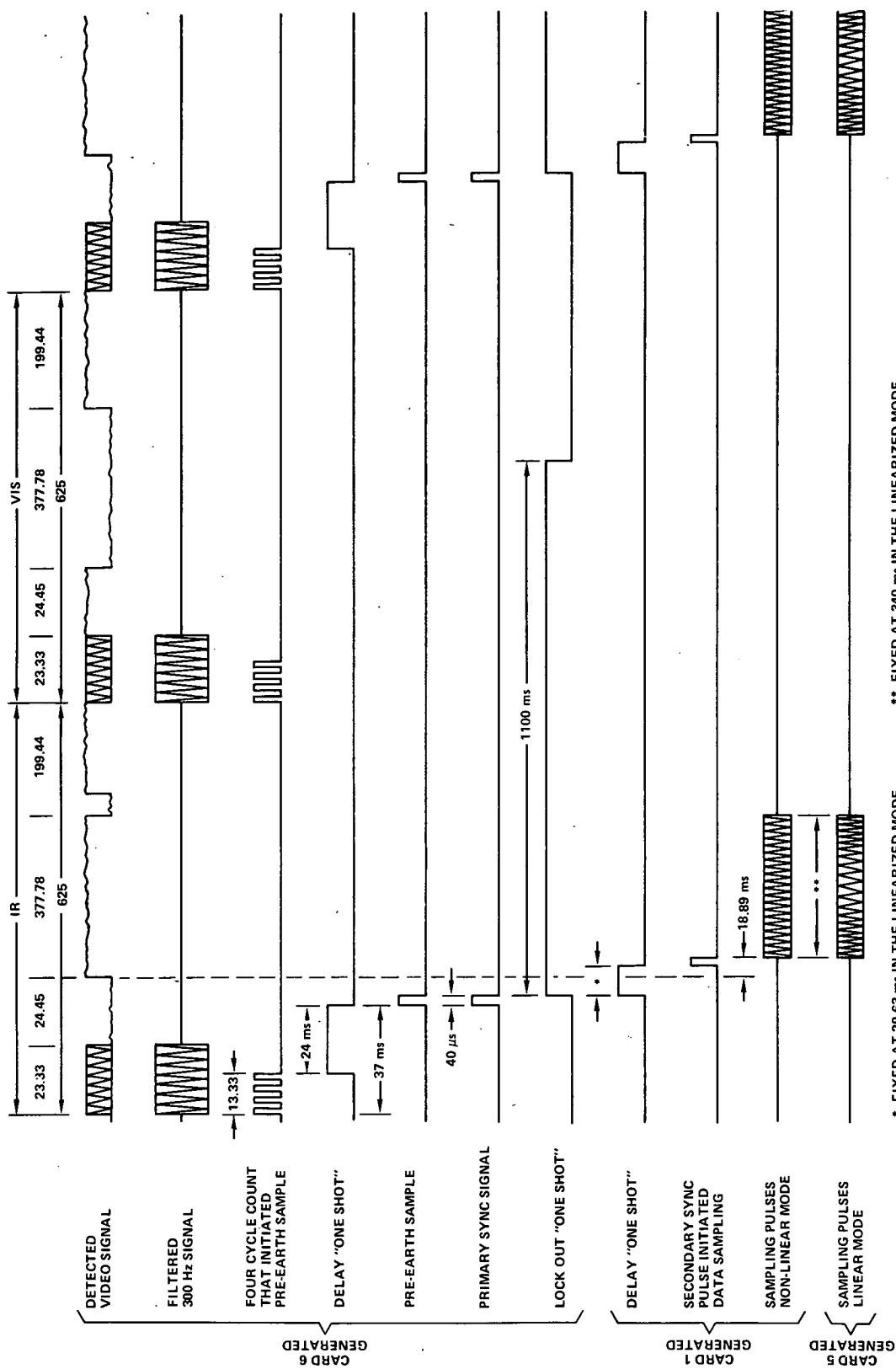


Figure 4. APT Digital Scan Converter, Functional Block Diagram

Card 6 demodulates the 2.4 kHz subcarrier, detects the 300 Hz sync bursts, generates a time delay suitable for pre-earth scan examination and generates a primary sync pulse which is sent to the Timing and Clock Pulse Generator Card (Card 1). The timing sequence of these events is shown in figure 5.

Simultaneously, the 2.4 kHz subcarrier is demodulated in the Analog Signal Processing and Amplitude Modulator Card (Card 4). The video is then amplitude-adjusted and filtered to eliminate any high frequency components which could cause aliasing in the digitizing process. The processed analog video is sent to the A/D portion of the Analog-to-Digital and Digital-to-Analog Converter Card (Card 3).



* FIXED AT 29.63 ms IN THE LINEARIZED MODE,
VARIABLE IN THE NON-LINEARIZED MODE.

** FIXED AT 340 ms IN THE LINEARIZED MODE,
VARIABLE IN THE NON-LINEARIZED MODE.

Figure 5. Sync Pulse Timing

The primary sync pulse enables the timer circuitry of Card 1. Card 1 generates a secondary sync pulse which enables the load and transfer oscillators. The outputs of these oscillators control the operation of the A/D portion of Card 3 and the transfer of data in and out of memory.

The Panoramic Distortion Correction Card (Card 5) generates a pulse train whose period for each pulse represents the same length of earth's surface. Therefore, by using this pulse train to control data sampling, correction for panoramic distortion is accomplished. Furthermore, when these samples are stored in memory, each scan line in memory is in a linear format.

The dump oscillator of Card 1 provides output data at a constant rate, compatible with the scan rate of the display monitor.

The digital data leave the Memory Buffer Card (Card 2) and enter Card 3 for Digital-to-Analog, D/A, conversion and are then forwarded to Card 4 for analog signal processing. In Card 4, the video is filtered. The processed video is then used to modulate a 2.4 kHz signal which is sent directly to the display monitor for observation and/or hard copy.

This 2.4 kHz signal may be an integral part of the scan converter or it may be brought in from an external source. Because the stability requirements of an oscillator are usually the determining factor on its cost, it is important to understand the requirements of this 2.4 kHz oscillator to determine the most cost effective option available. More stringent requirements of the 2.4 kHz oscillator are shown in Appendix E, Power Supplies/Precision Clock.

Circuit Descriptions

The descriptions of the circuits are arranged in a card order which follows the logical signal flow through the system.

Sync Pulse Generator Card (Card 6)

Figure 7 is a schematic diagram for Card 6. The Sync Pulse Generator (Card 6) provides a reference sync pulse from which scan angle θ can be determined (figure 5). To achieve this function, Card 6:

1. Detects and isolates the 300 Hz burst contained in the video data received from the scanning radiometer,
2. Determines if the subsequent scan will be infrared (IR) or visible (VIS),
3. Rejects spurious 300-Hz signals, and
4. Produces the sync pulse.

Brief Circuit Description

Two bursts of seven cycles of 300 Hz are provided twice each sweep from the scanning radiometer. One burst precedes the IR scan and the other burst precedes the VIS scan. The bursts occur when the scanner is at right angles to a line from the spacecraft to nadir. This angle is shown in figure 6 as λ , and the bursts which define this angle are used as the references from which angle θ is determined.

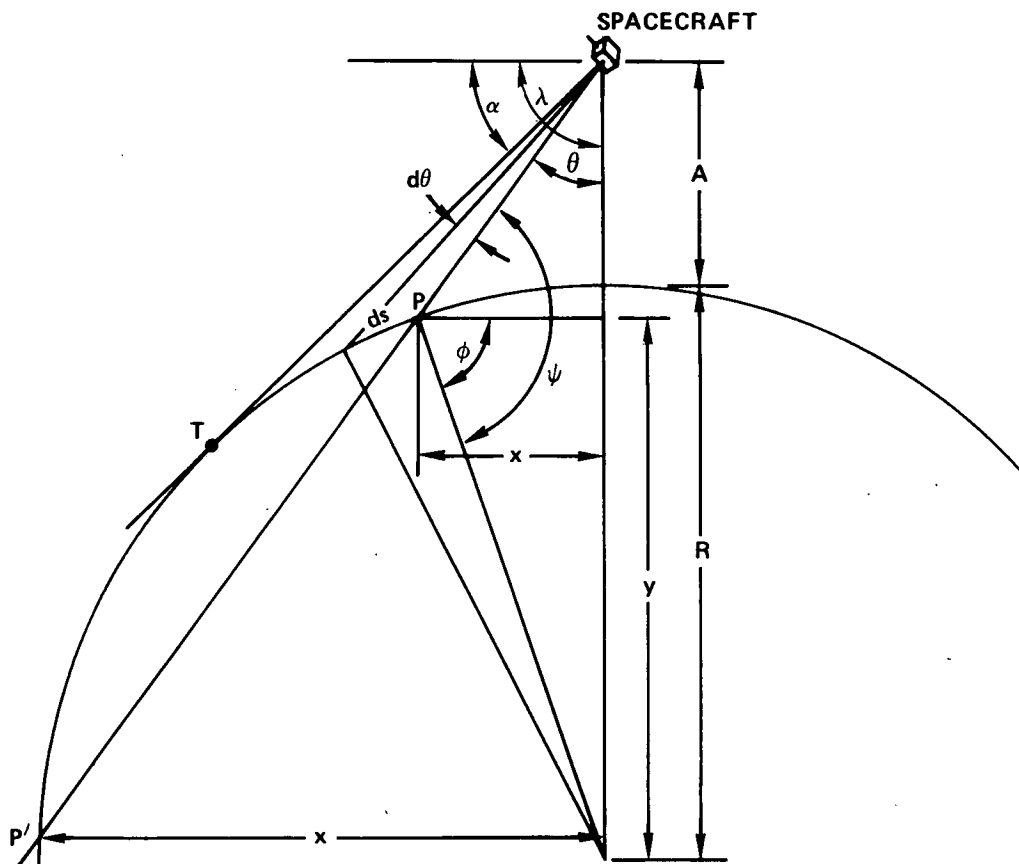


Figure 6. Spacecraft and Earth Geometry

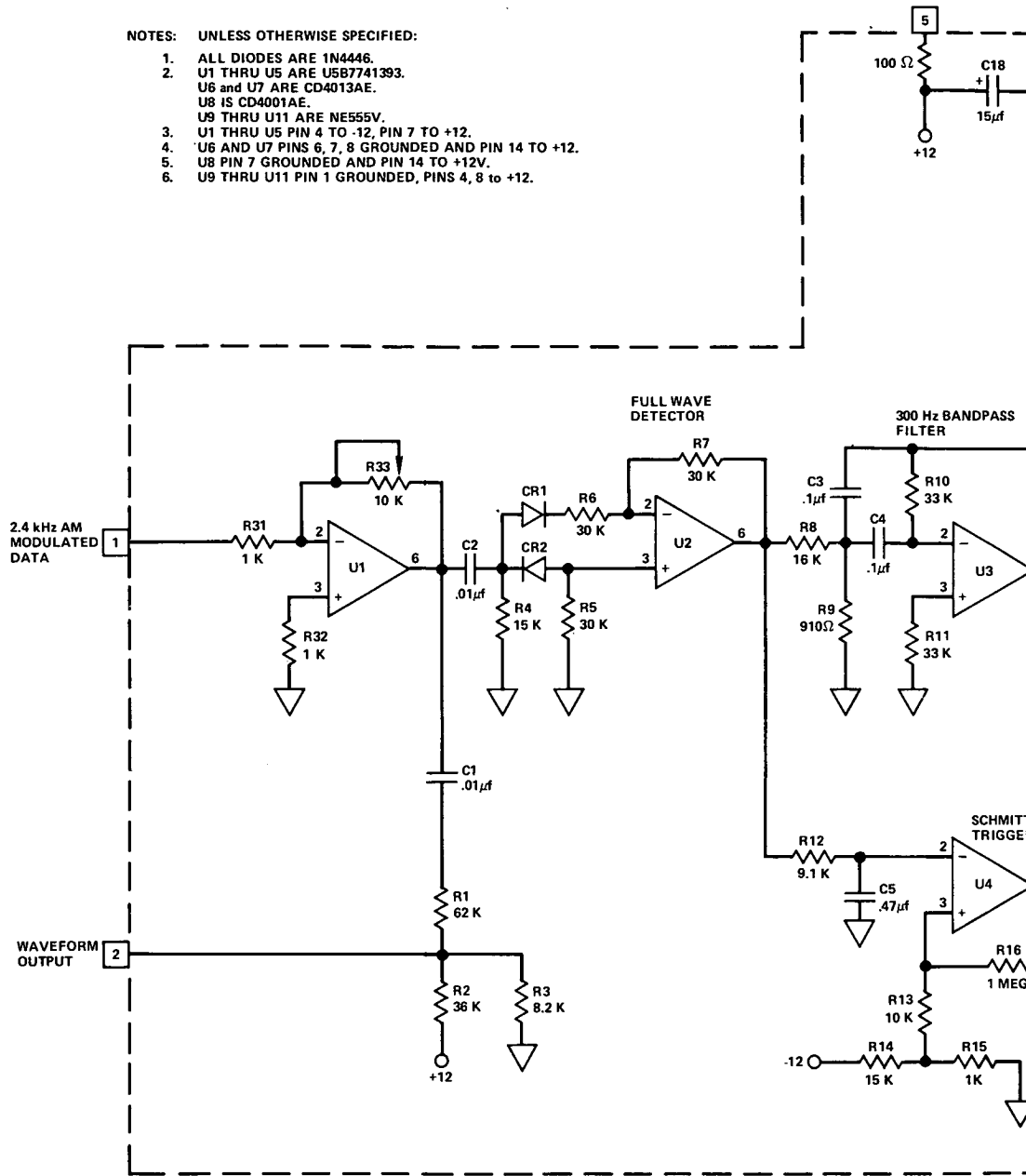
Detailed Circuit Description

The video input (2.4 kHz AM subcarrier at pin 1 of Card 6) is amplified by U1 and demodulated by the full-wave detector circuit (figure 7) containing CR1 and CR2 and amplified by U2. The signal then passes through a 300 Hz bandpass filter (U3) isolating seven cycles (1 burst) of the 300 Hz sync signal. The 300 Hz burst is then peak detected and squared by Schmitt Trigger U5 whose output drives a straight binary counter consisting of U6 and one half of U7. On the fourth count, delay one-shot U10 is triggered which resets the counter and Schmitt Trigger and provides the sample pulse for sync pulse generator U7B.

The demodulated signal from U2 also passes through a 30 Hz low-pass filter (R12 and C5) and is squared by Schmitt Trigger U4. In addition, this circuit sets the threshold to determine the presence of black or white in the video signal during the interval that the scanner is looking at space (figure 6, angle α). Sync pulse generator U7B generates a 40 μ s sync pulse if the data input line, via the IR/VIS switch, is at a high level when the sample pulse is applied from U10. The resulting sync pulse is applied to pin 14 of Card 6. It is then inverted and applied to the one-shot, U11, which, when triggered, holds the divide-by-four counter in a reset state for approximately 1100 ms until the next sync burst is applied to the counter. This prevents false triggering of the counter by noise associated with the 300 Hz signal. At the end of this period, one-shot U9 provides a reset pulse to reject any false counts occurring before the start of the next sync burst. This circuit functions as a retriggerable one-shot that generates a reset pulse only when the period between trigger pulses exceeds 4.5 ms.

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL DIODES ARE 1N4446.
2. U1 THRU U5 ARE U587741393.
U6 AND U7 ARE CD4013AE.
U8 IS CD4001AE.
U9 THRU U11 ARE NE555V.
3. U1 THRU U5 PIN 4 TO -12, PIN 7 TO +12.
4. U6 AND U7 PINS 6, 7, 8 GROUNDED AND PIN 14 TO +12.
5. U8 PIN 7 GROUNDED AND PIN 14 TO +12V.
6. U9 THRU U11 PIN 1 GROUNDED, PINS 4, 8 TO +12.



REFERENCE DESIGNATION LAST USED

R33 CR8 U11 Q1 C19

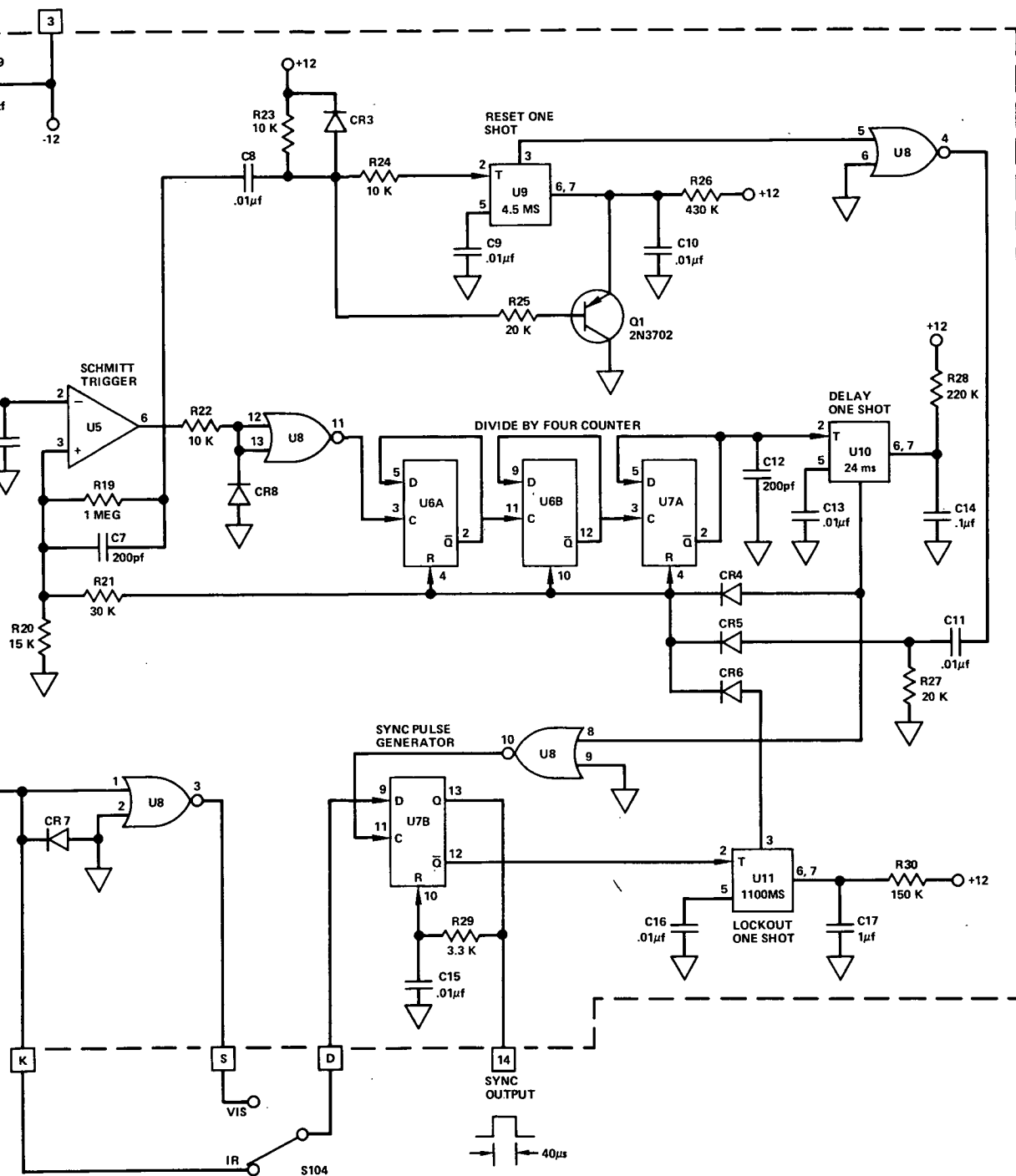


Figure 7. Sync Pulse Generator Card (Card 6), Schematic Diagram

Panoramic Distortion Correction Card (Card 5)

Figure 13 is a schematic diagram for Card 5.

The Panoramic Distortion Correction Card (Card 5) corrects panoramic distortion associated with the incoming NOAA-3 or NOAA-4 signal. This correction is accomplished by generating a curve which is proportional to the rate change of earth's surface relative to the angular velocity of the scanning radiometer. A detailed discussion of this nonlinearity is contained in Appendix A.

Brief Circuit Description

The correction curve is generated by using three fundamental building blocks: a ramp generator, a diode shaper, and a voltage controlled oscillator. The ramp generator generates a linear ramp from 10.3 volts at the beginning of the scan representing the left extremity of the sweep to 0 volts at midpoint or nadir, back to 10.3 volts at the right extremity of the sweep. The time duration of the sweep from one extreme to the other is 340 ms (figure 8). This signal is then processed through a diode shaper to form the curve shown in figure 9. This function, when applied to the Voltage Controlled Oscillator (VCO), generates an output frequency proportional to the input voltage. The result is a frequency vs. time curve which represents the rate change of earth's surface with respect to the angular change of the scanning radiometer. After processing, each pulse period at the output of the VCO is equal to the same distance of the earth's surface. Each pulse of this pulse train is shaped and sent to the Timing and Clock Pulse Generator Card (Card 1).

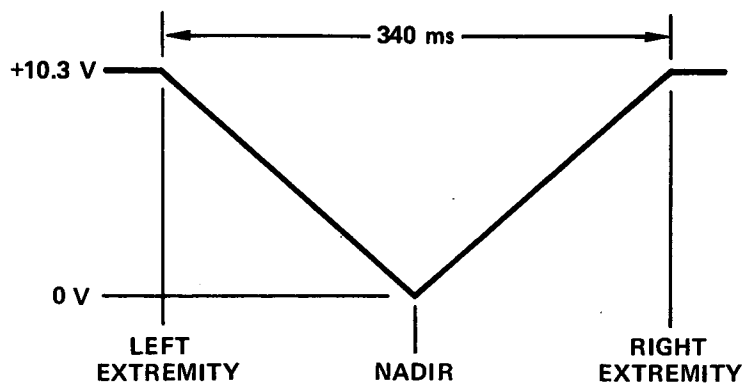


Figure 8. Sweep Timer Duration

Detailed Circuit Description

The modified sync signal from Card 6, pin 14 enters Card 5 at pin 3 (figure 13) and is shaped by capacitors C1 and C2, and resistors R7 and R8 and applied to the base of transistor Q2. Transistor Q2 acts as a shorting switch across capacitor C3 of the sweep generator.

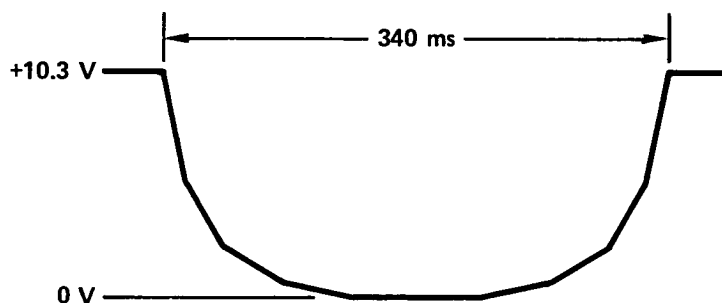


Figure 9. Curve Processed Through Diode Shaper

The rate at which capacitor C3 charges is a function of voltage applied to resistor R6 through resistor network R3, R4, and R5. Zener diode LVA68A limits the output of amplifier U1A (figure 10) to 6.8 volts. Control R4 adjusts the slope of the ramp such that the output voltage of U1A goes from 0 to 6.8 volts in 340 ms. U1B is an offset amplifier that amplifies and equally balances the 6.8 volt sweep above and below ground. The gain of amplifier U1B is determined by resistors R11 and R14 and is approximately 3. The output of amplifier U1B, therefore, swings 20.6 volts with a 6.8 volt input. Resistor R13 provides the offset current that adjusts the output of amplifier U1B to swing from -10.3 volts to +10.3 volts when the output of amplifier U1A (pin 12) swings from 6.8 to 0 volts (figure 11).

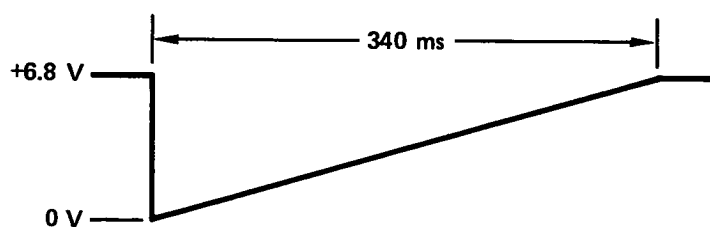


Figure 10. Output of Amplifier U1A

The function of amplifier U2A is to rectify the output of amplifier U1B. The gain of amplifier U2A is set by resistors R16 and R18 to unity as pin 10 of amplifier U1B goes positive. The gain of amplifier U2A is 0 as pin 10 of amplifier U1B goes negative. The output of amplifier U2B is shown in figure 12. Amplifier U2B sums the output of amplifiers U1B and U2A through resistors R19, R20, and R21. The gain of amplifier U2B is unity through resistors R19 and R21 and the gain is two (2) through resistors R20 and R21. The output of amplifier U2B is the sum of these two input currents. The output of amplifier U2B is fed into a diode shaping network. The method for determining the values of the resistors in this network is shown in Appendix B.

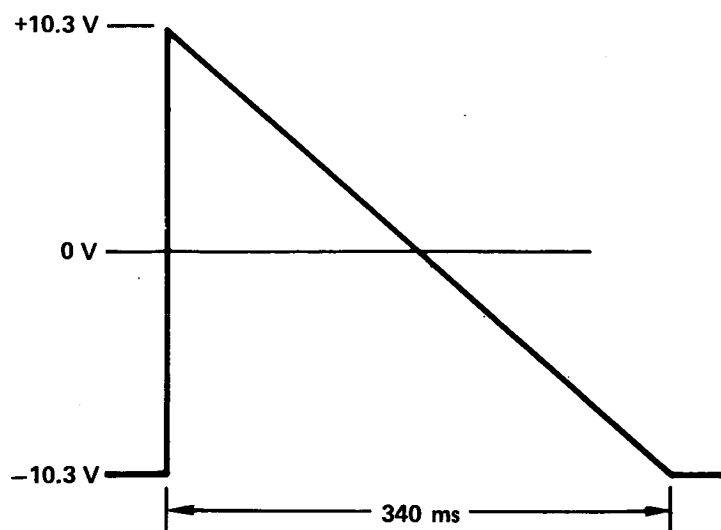


Figure 11. Offset Current Which Adjusts Output of Amplifier U1B

Consistent with the operation of a summing amplifier, pin 1 of amplifier U3A is essentially at ground potential and all current out of the resistor diode network sums through resistor R33. Diodes CR5, CR4, CR3, and CR6 switch-in resistor networks R29-R30, R27-R28, R25-R26, and R23-R24 which provide voltages 2.409 volts, 5.18 volts, 7.409 volts and 9.276 volts, respectively. The currents are summed from these diodes to form the output of amplifier U3A which is provided directly into One-to-One Inverter U4A whose output is shown in figure 9. Amplifier U4B is a summing amplifier that scales the output correction curve to the rate change of the earth's surface with respect to the angular velocity of the scanning radiometer of the satellite. As shown in Appendix B, the ratio of the maximum current through resistor R34 and the current through resistor R36 should be 4.69 to 1. These currents are summed through resistor R38, allowing a maximum voltage output of approximately -10 volts at amplifier U3B. Amplifiers U5A and U5B combine to form the Voltage Controlled Oscillator and Gate. Amplifier U5A is a standard integrator circuit whose charging capacitor is shunted by transistor switch Q3. Amplifier U5B is a zero-crossing detector and gate whose output is connected to transistor Q3. Since amplifier U5A is a high-gain amplifier, it is reasonable to assume that all current through resistors R35 and R40 goes through capacitor C5. Since pin 1 of amplifier U5A is assumed to be ground potential, a constant voltage at the output of amplifier U4B, pin 10, will produce a constant current through resistors R35 and R40. This constant current through capacitor C5 produces a linear voltage buildup across C5. The output of amplifier U5A is fed through the voltage divider resistors, R44 and R46, to pin 6 of amplifier U5B. As pin 6 of amplifier U5B crosses zero in the positive direction, pin 10 of amplifier U5B goes to saturation in the positive direction, applying this voltage to the base of transistor Q3 through resistor R42

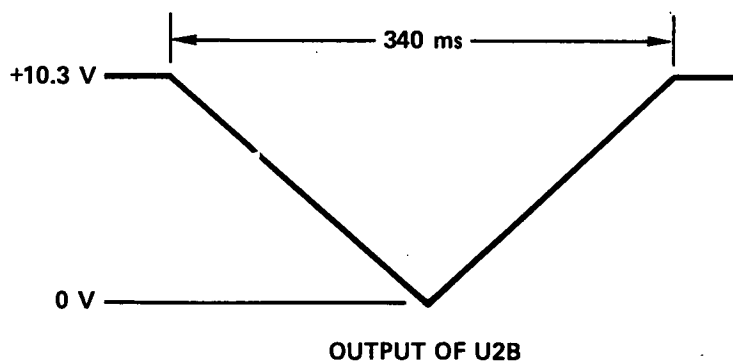
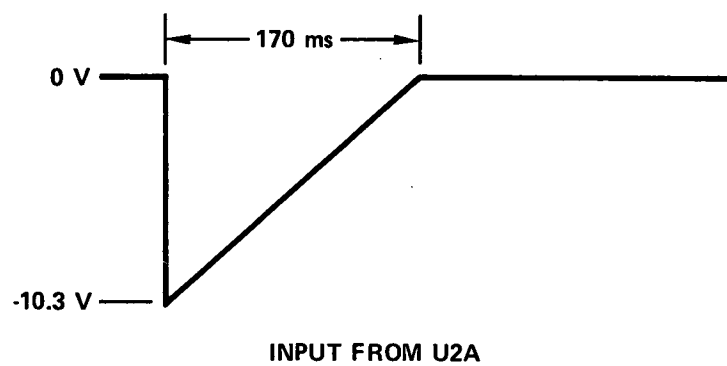
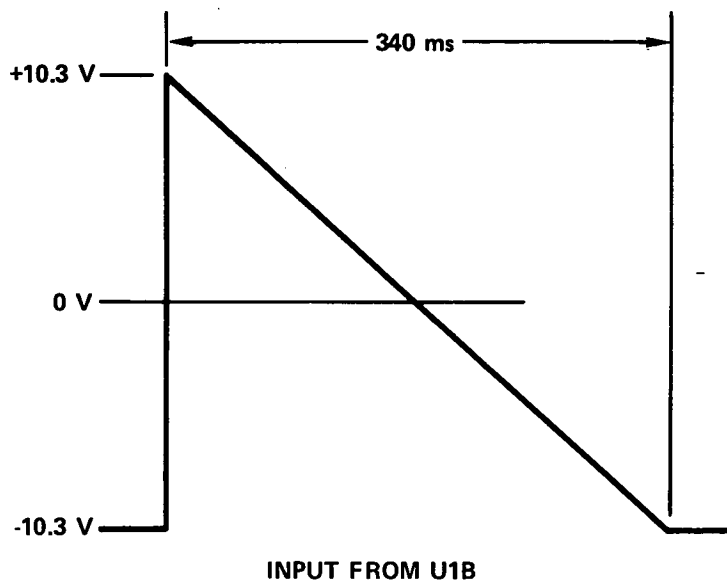
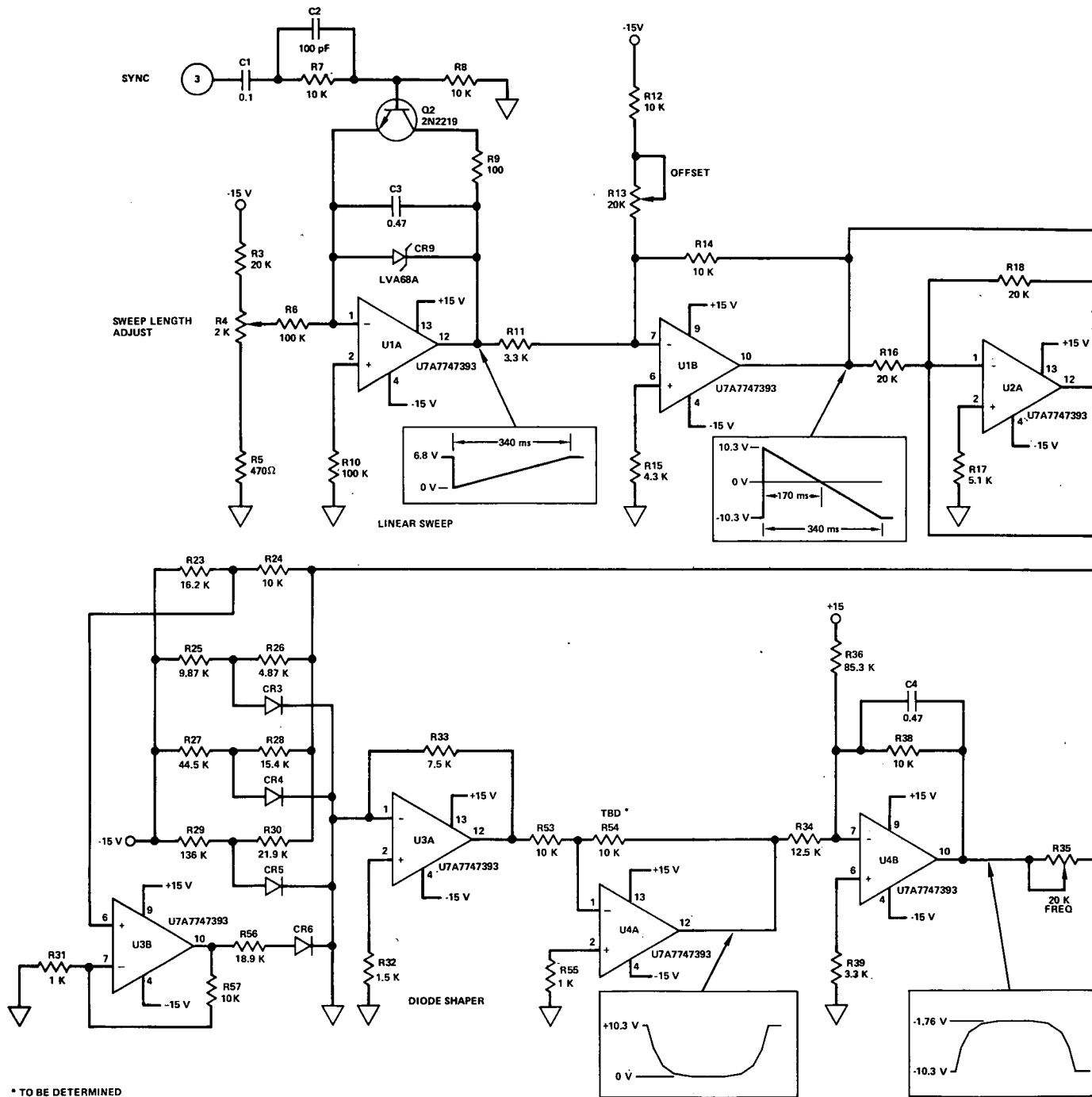


Figure 12. Output of Amplifier U2B

and reinforcing the input at pin 6 of amplifier U5B through resistor R45. Resistors R58, R47, and R57 and diodes CR7 and CR8 are the gating components which enable the Voltage Controlled Oscillator. Diode CR8 allows pin 6 of amplifier U5B to go from -15 volts to approximately +0.5 volt. When the voltage above 3 volts is applied to pin 12 of Card 5, pin 7 of amplifier U5B is biased above the positive 0.5 volt maximum which may be found on pin 6 of amplifier U5B. Therefore, amplifier U5B, pin 10, stays low or at -15 volts for any voltage from -15 to +15 volts at the output of amplifier U5A, pin 12. With V/F control voltage present at pin 12 of Card 5, the output of amplifier U5A is at positive saturation. When the V/F control voltage is removed from pin 12 of Card 5, pin 7 of amplifier U5B is at ground potential. Pin 12 of amplifier U5A goes to positive saturation which enables transistor Q3 and oscillation begins.

Timer/Delay U6 is a one-shot multivibrator that shapes the output of amplifier U5. This shape pulse train is then fed through pin 20 of Card 5.



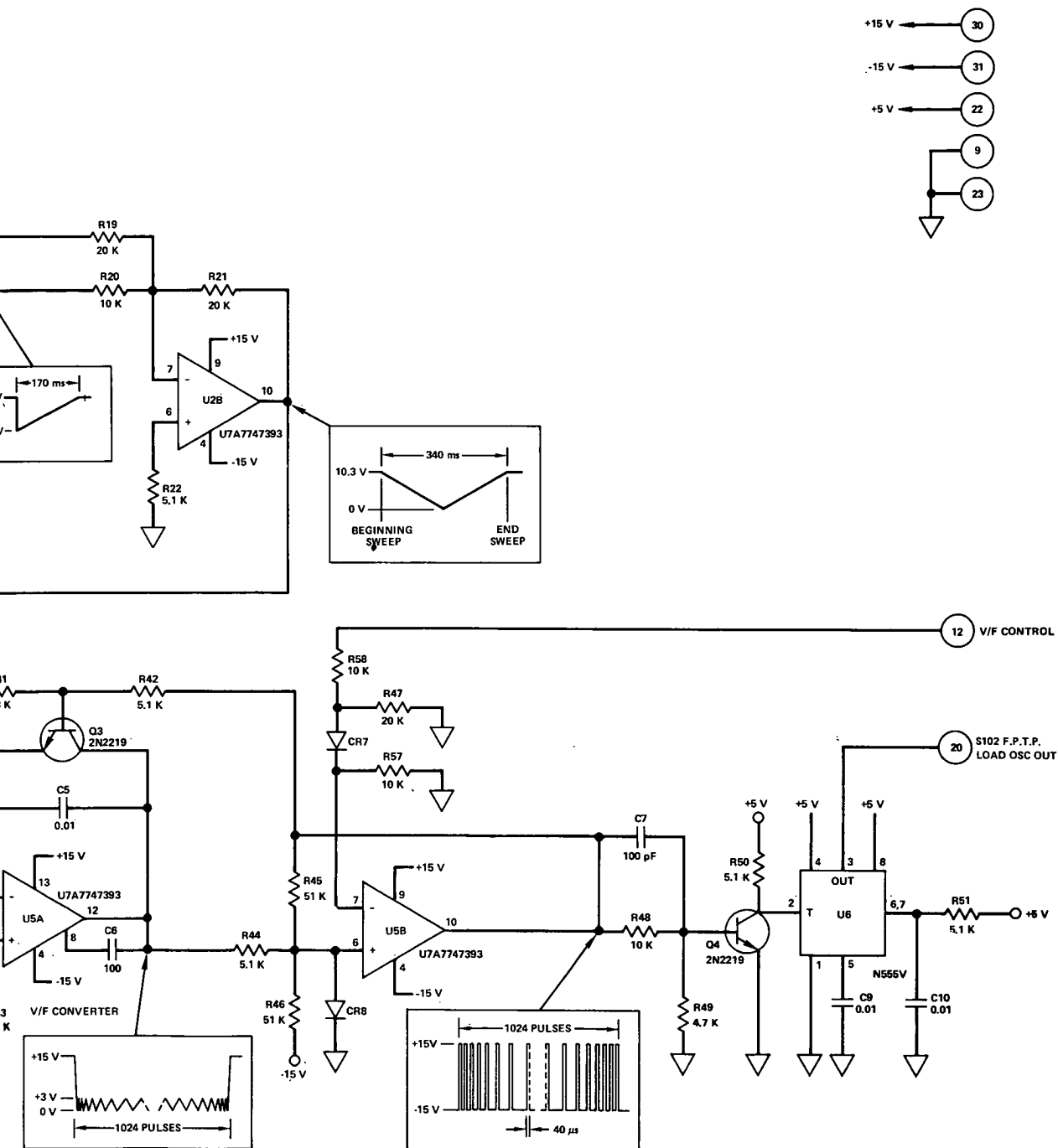


Figure 13. Panoramic Distortion Correction Card (Card 5), Schematic Diagram

Analog Signal Processing Card (Card 4)

Figure 18 is a schematic diagram for Card 4.

The Analog Signal Processing Card (Card 4) amplifies, filters, and demodulates the incoming 2.4 kHz subcarrier and conditions the detected video for the analog-to-digital conversion. This card also receives video from the Digital-to-Analog, D/A, portion of Card 3 and amplitude modulates the 2.4 kHz carrier.

Brief Circuit Description

The 2.4 kHz subcarrier is first processed by a single-pole low-pass filter with a 3 dB point at 6.8 kHz. This signal is detected with a precision full-wave rectifier and filtered by a two-pole Butterworth filter to remove the rectified carrier. The video is then amplified by a variable gain filter which uses an offset current to provide contrast and black-level controls.

The video leaves Card 4 for digital processing. After the digital processing is performed and the processed video returns, it uses an operational/amplifier-chopper/modulator to modulate a 2.4 kHz signal. The remodulated signal is then filtered to suppress the high frequency components generated by the chopping action.

Detailed Circuit Description

The modulated subcarrier is applied to Card 4 at pin 18 (figure 18). Capacitor C1 eliminates any d.c. voltage in the 2.4 kHz input signal. Resistor R1 is a gain control which is adjusted to ensure that subsequent amplifier stages are not operating in saturation. Amplifier U1A is a single-pole low-pass filter amplifier with a gain of two (2) and a bandpass of 6.1 kHz. Amplifiers U2A and U2B form a precision full-wave rectifier used as a demodulator. Amplifier U2A half-wave rectifies and amplifies the output of amplifier U1A at pin 12 without the distortion normally accompanying diode switching at low levels.

As the output of amplifier U1A at pin 12 goes positive, the output of amplifier U2A swings negative, passing the current of resistor R4 through diode CR2. The output voltage of amplifier U2A at pin 12 is a negative voltage equal to the drop across diode CR2 in the forward direction (approximately 0.5 volts). Diode CR1 is back-biased and therefore not conducting current. The potential at the cathode of diode CR1 is essentially the same as that of pin 1 of amplifier U2A which is essentially at ground potential.

As the output of amplifier U1A at pin 12 goes negative, the output of amplifier U2A at pin 12 goes positive. Since pin 1 of amplifier U2A is essentially at ground potential, diode CR1 is forward-biased, diode CR2 is back-biased, and the gain of the amplifier, set by resistors R4 and R5, is two (2).

Amplifier U2B is a one-to-one summing amplifier which sums the output voltage of amplifier U1A at pin 12 and the voltage at the cathode of diode CR1. Figure 14 shows how these two voltages result in full-wave rectification.

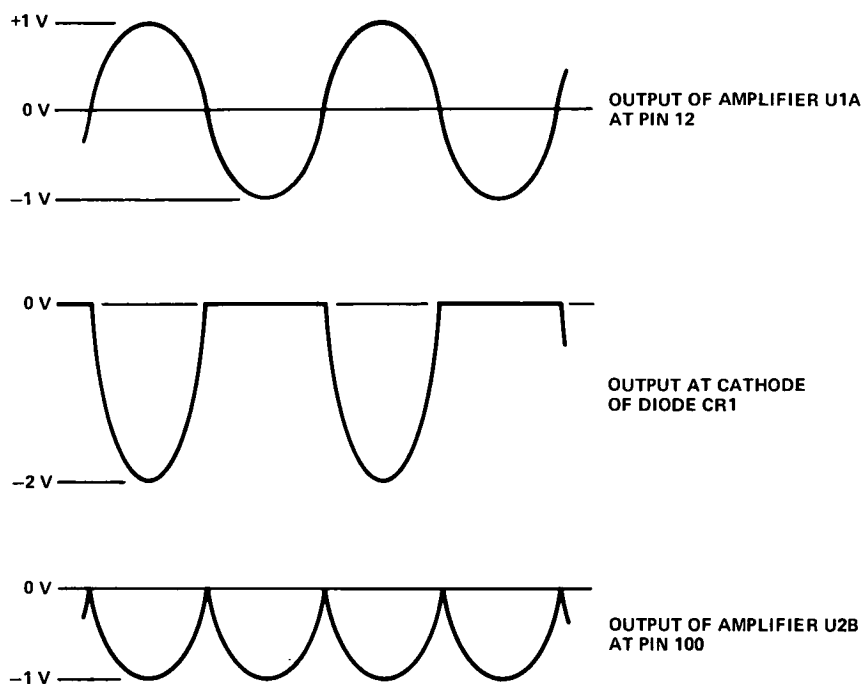


Figure 14. Output Voltage Summing Resulting in Full-Wave Rectification

It may be necessary to adjust the value of R5 such that the gain of amplifier U2A is exactly two (2).

The output of amplifier U2B is applied to a two-pole Butterworth filter of amplifier U3A. Its characteristics are shown in figure 15.

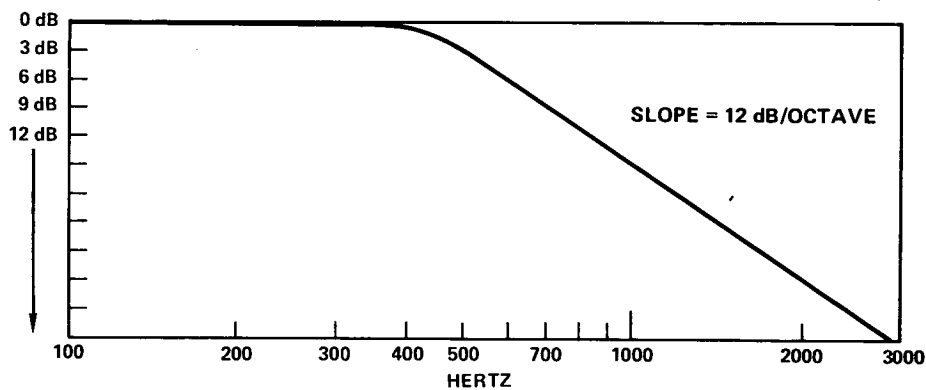


Figure 15. Characteristics of Amplifier U2B Output

The 3 dB cutoff frequency of the filter was selected at 511 Hz which optimized the quality of both IR and VIS data. Five hundred eleven (511) Hz is well above the satellites' 450 Hz bandpass in the IR and improves the signal-to-noise ratio of both the IR and VIS data. This is accomplished with little or no deterioration of the VIS modulation transfer function.

Amplifier U3B is a variable gain amplifier. Its gain is adjusted by potentiometer R115. The gain is determined by resistor R14 and potentiometer R115 and is variable from 0 to 20. Potentiometer R116 is connected between -15 volts and +15 volts and is the voltage source from which offset current is provided to alter the black level of the incoming signal. The video is sent to the analog-to-digital, A/D, portion of Card 3 through pin 13 of Card 4.

The processed video is returned to Card 4 through pin 32 to resistor R24 which is a gain control through which the output of amplifier U1B can be adjusted for optimum performance. Amplifier U1B has a gain of three (3) which is determined by resistors R25 and R21. The processed video from amplifier U1B is provided to modulator U4A.

At pin 33, a 2.4 kHz signal enters and is applied to the base of transistor Q1 through capacitor C7, resistor R18, and resistor R22. Transistor Q1 acts as a switch which shorts pin 6 of amplifier U4A to ground when turned on. When pin 6 is at ground, amplifier U4A is an inverting one-to-one amplifier in which the output is the inverse of the input. When transistor Q1 is open, pins 6 and 7 of amplifier U4A are at the same potential as the output of amplifier U1B and consequently, amplifier U4A acts as a positive voltage follower in which the output is equal to the input. Notice that the output of amplifier U4A is a modulated 2.4 kHz signal if the output of amplifier U1B is always positive and contains frequencies of less than one-half of the clock frequency (figure 16).

Amplifier U4B is a two-pole low-pass Butterworth filter with a 3 dB point at 5.7 kHz. This stage suppresses the high frequency components of the chopped modulated signal of amplifier U4A (figure 17).

R38 protects the output of amplifier U4A against short circuits and R39 provides a variable output adjusted to match the input voltage requirements of the display monitor.

The modified video is sent to the video out jack, J103, on the rear chassis assembly.

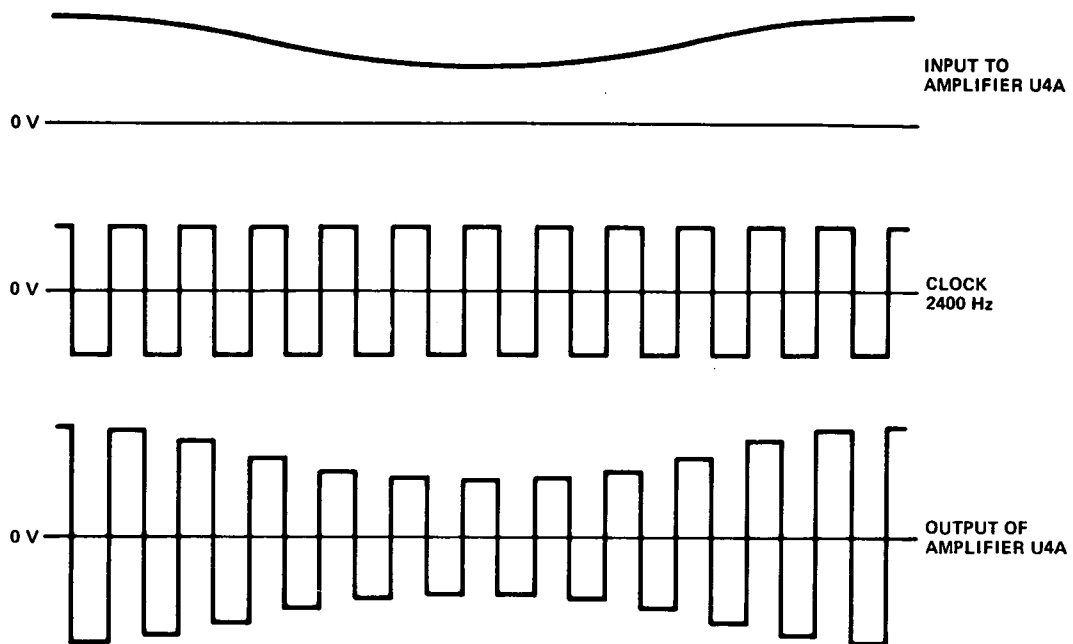


Figure 16. Clock Frequency Relationship of Amplifier U4A Input/Output

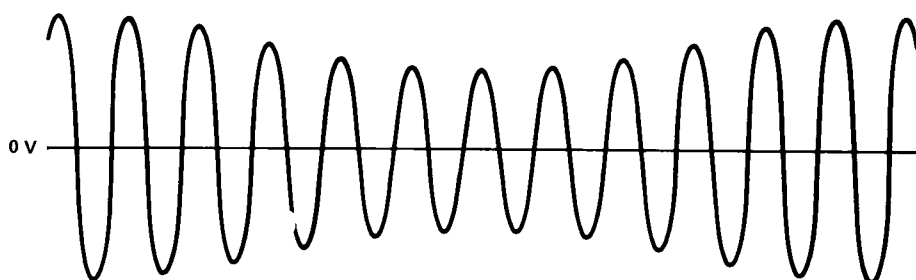
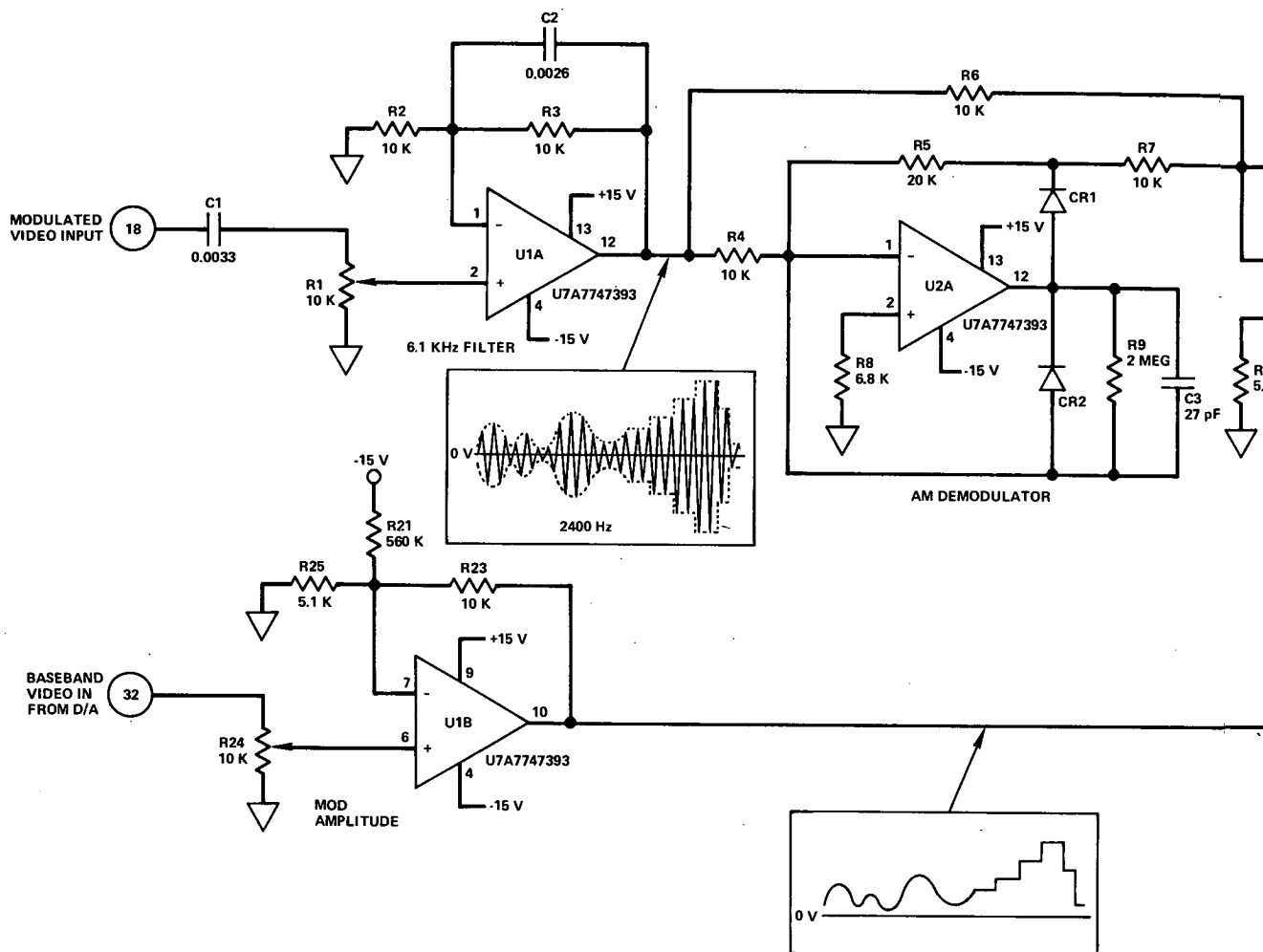


Figure 17. Chopped Modulated Signal of Amplifier U4A



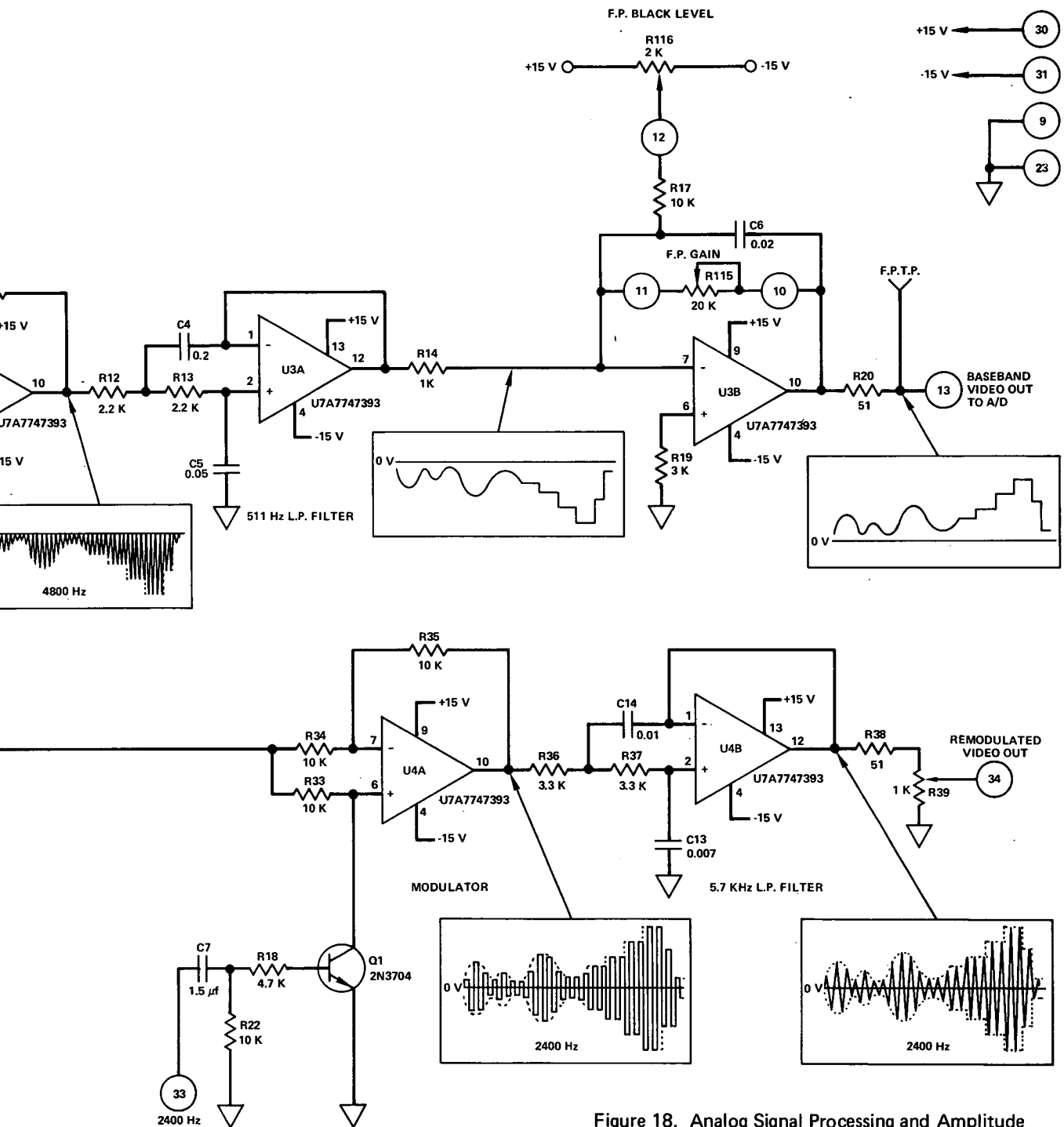


Figure 18. Analog Signal Processing and Amplitude Modulation Card (Card 4), Schematic Diagram

Analog-To-Digital and Digital-To-Analog Converter Card (Card 3)

Figure 19 is a schematic diagram for Card 3.

The Analog-to-Digital and Digital-to-Analog Converter Card (Card 3) performs the analog-to-digital, A/D, and digital-to-analog, D/A, conversion functions.

Brief Circuit Description

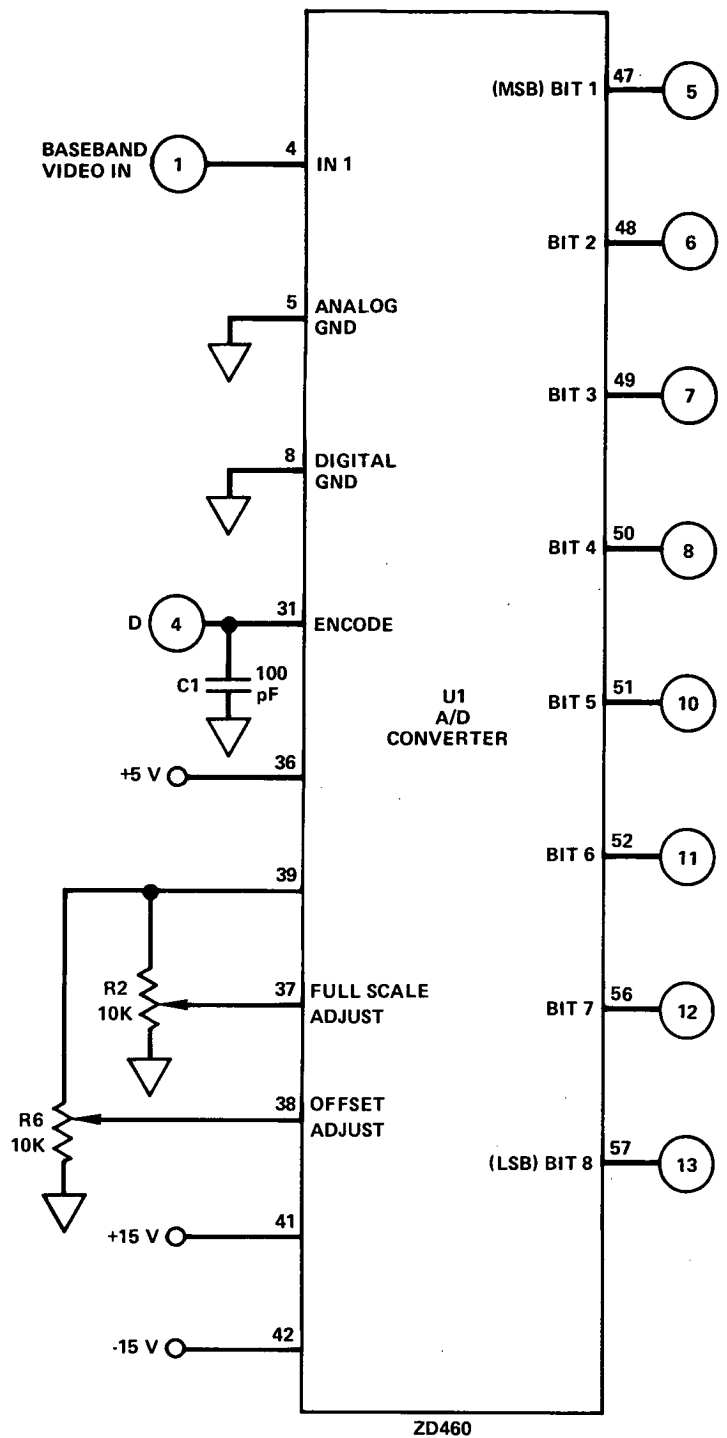
Because the Detailed Circuit Description is brief in itself, this section is left blank intentionally.

Detailed Circuit Description

Card 3 possesses two independent converter circuits. One is the analog-to-digital (A/D) circuit and the other is the digital-to-analog (D/A) circuit.

The video from the Analog Signal Processing Card (Card 4) is digitized by the analog-to-digital converter into 8-bit words at a rate determined by the frequency set on the load clock of the Memory Buffer Card (Card 2) which will be approximately 3.0 kHz. Each conversion requires approximately 40 μ s to complete, which is more than adequate for this application. The analog-to-digital converter is calibrated so that a 0 to +10 volts range represents a binary output from 0 to 255. The output may be monitored on pins 5 through 8 and 10 through 13 of Card 3. Pin 5 is the most significant bit (MSB) and pin 13 the least significant bit (LSB). The logic is positive and therefore, a binary "1" is represented by a high voltage and a binary "0" is represented by a low or zero voltage. This digitized video is sent in parallel word format to the Memory Buffer Card (Card 2).

The processed digitized video is received from the memory buffer (card 2) via pins 14 through 21, with pin 14 representing the MSB and pin 21 representing the LSB. This parallel word format to the digital-to-analog converter, converts bits 1 through 8, and is provided at pin 15 of U2 as an analog voltage calibrated from 0 to 1 volt for a binary input of 0 to 255. This output is applied to the non-inverting amplifier U3 which has a gain of ten (10) determined by resistors R4 and R5. The output, therefore, goes from 0 to 10 volts for an input of 0 to 1 volt. Amplifier U1 also is a single-pole low-pass filter with a 3 dB point at 1.7 kHz. The output of amplifier U1 is sent via pin 25 of Card 3 to the Analog Signal Processing Card (Card 4).



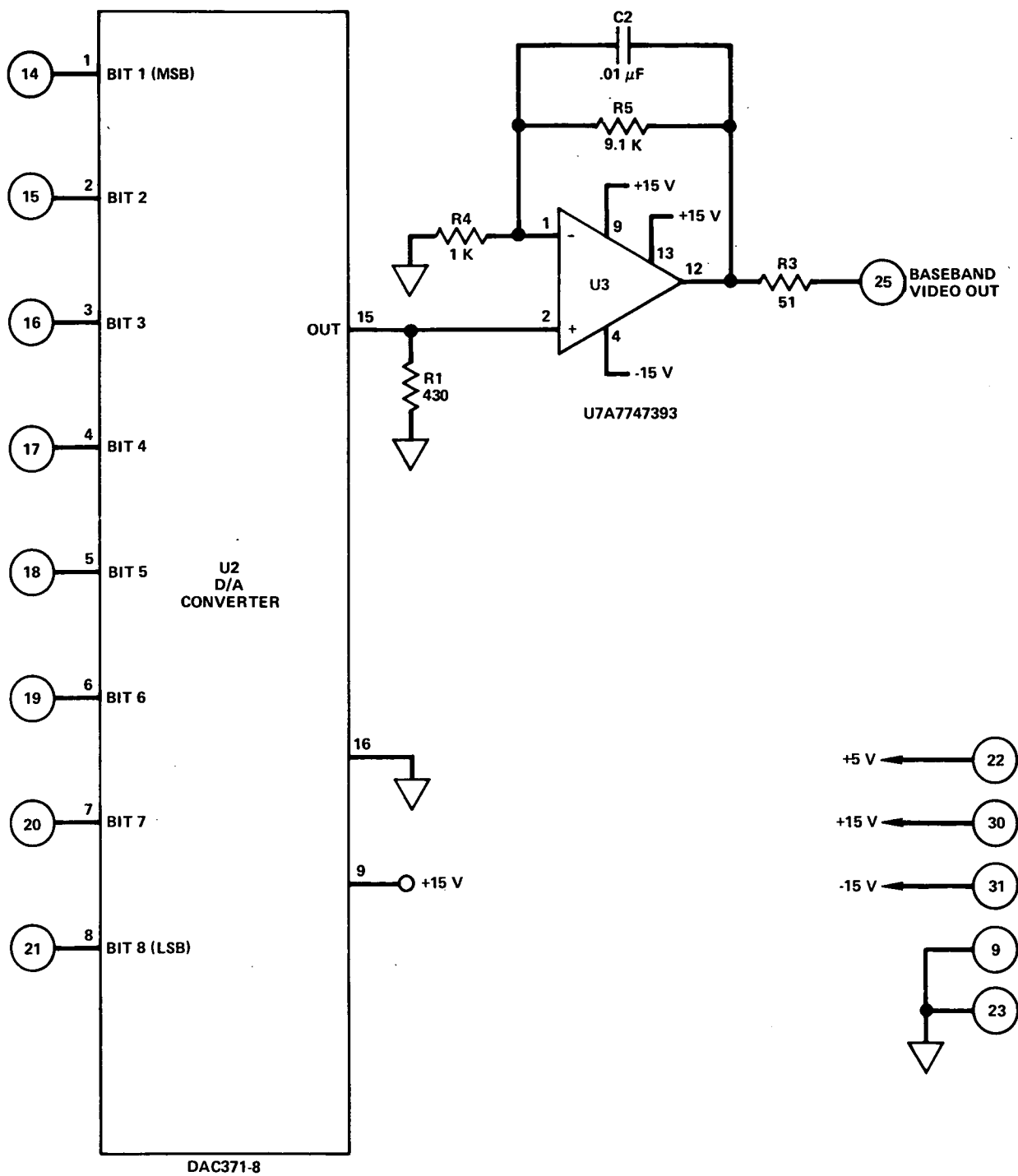


Figure 19. Analog-to-Digital and Digital-to-Analog Converter Card (Card 3), Schematic Diagram

Memory Buffer Card (Card 2)

Figure 22 is a schematic diagram of Card 2.

The Memory Buffer Card (Card 2) serves two functions: (1) to convert the 48 line per scan radiometer data to be compatible with the scan rate of the output display equipment at the APT ground station, and (2) to correct the panoramic distortion contained in the radiometer scan images. Achievement of the latter function requires use of the timing functions of Cards 1 and 5.

Brief Circuit Description

The buffer consists of three independent 8-bit, 1024-word memories referred to as Buffers A, B, and C. Buffer A is controlled by two sets of clock pulse trains, the load-clock pulse trains and the transfer-clock pulse trains (figure 20). The data are provided to this buffer in a parallel format from the analog-to-digital (A/D) portion of Card 3. Buffer A is connected in a pipeline configuration and as such, new words put into memory wipe out the last word in memory. The load- and transfer-pulse trains of Buffer A are asynchronous with the dump operation of Buffers B or C and therefore transfers its data totally independent of the operations of Buffers B and C.

Buffers B and C are also controlled by two sets of clock-pulse trains, the transfer-clock-pulse train and the dump-clock pulse train. The operational difference between Buffer A and Buffers B and C is that Buffer A will accept either of the two pulse-trains while Buffers B and C will accept only one each of the two pulse-trains (that is, when Buffer B is accepting the transfer clock-pulse trains, then Buffer C will accept only the dump-clock pulse train, and vice versa). Register-Select signals determine which buffer will dump and which one will accept clock-pulse trains for the next data transfer from Buffer A.

Because (1) the dump clock pulses are set at a rate slightly less than the scan rate of the display monitor (1024 pulses per scan), and (2) data transfer is performed completely independent of the dump function, two dump buffers are required. When Buffer B is operating as the standby buffer ready to accept data from Buffer A (data transfer cycle), Buffer C is performing the dump function on the last scan line of data received. Once Buffer B is filled with new data and Buffer C has completed dumping a complete line of data, Buffer B assumes the role of the dumping-buffer and Buffer C becomes the standby-buffer. This toggling action between Buffers B and C continues until the last line of data is transferred. At that time, the buffer that last assumed the dumping function will continue dumping the same data until new data are inserted or the machine is turned off.

Detailed Circuit Description

The load- and transfer-pulses enter Card 2 at pin 10 (figure 22). The 8-bit data word is applied to pins 1 through 8 with the most significant bit (MSB) being on pin 1 and the least significant bit (LSB) being on pin 8. U1 through U8 are Metal Oxide Silicon, MOS, type

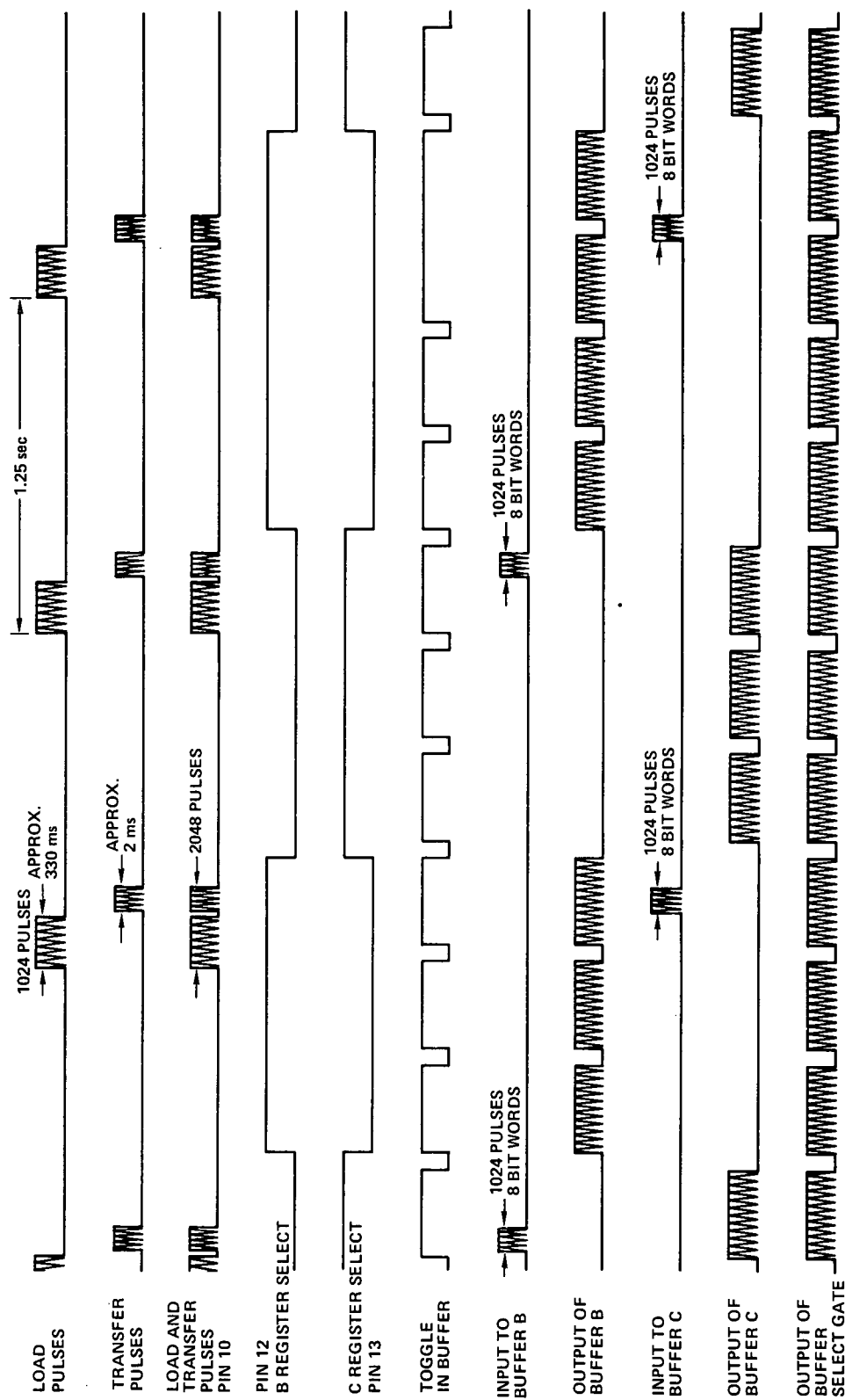


Figure 20. Memory Buffer Circuit Timing Diagram

shift registers, constructed in a 1-bit by 1024-stage format. On each register, the input bit is applied to pin 5, the shifting clock pulse to pin 6 and the output in on pin 7. The registers are enabled by applying +5 volts to pin 3 and disabled when pin 3 is at or near zero voltage potential. In Buffer A, pin 3 of all registers is at ground potential and therefore the register will shift on command by either the load-or the transfer-clock pulses.

Buffers B and C are configured so that each register may either accept new data at pin 6 or recirculate old data through pin 7. When pin 3 is at logical "1", data circulate from pin 1 to pin 7 through the register again to pin 1; this process is in synchronization with the clock-pulses at pin 6. When pin 3 is at logical "0", the data at pin 5 are entered into the register and the data at the output (pin 1) are lost.

The Register-Select signals enter Card 2 through pins 12 and 13. The Register-Select signals B and C toggle, first having pin 12 at logical "1" and pin 13 at logical "0" and vice versa. The purpose of the Register-Select signals is to select which Buffer (B or C) will operate as the Standby-Buffer and which one as the Dump-Buffer.

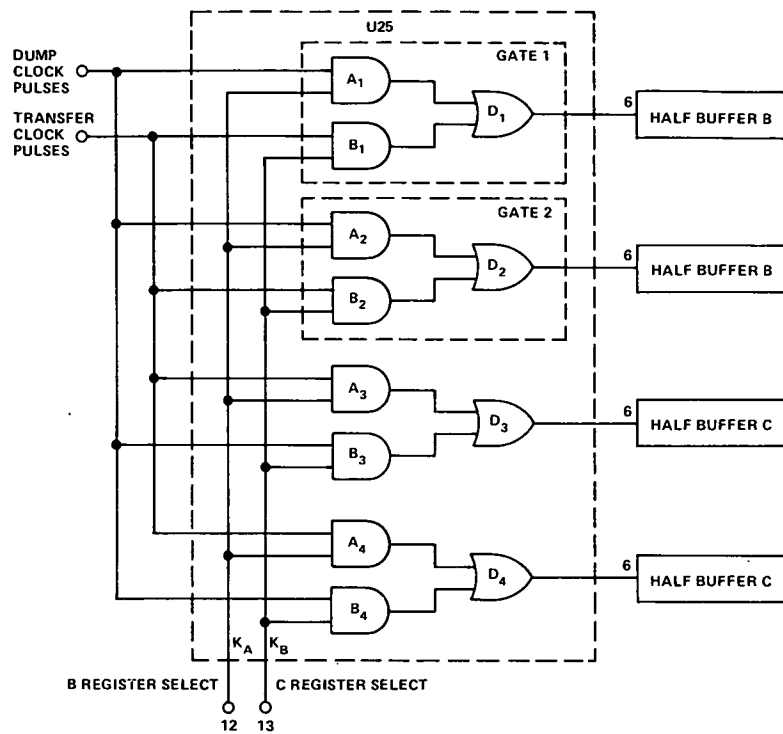
U25, U26, and U27 are gates configured as shown in figure 21. Figure 21A shows the connection of U25 into the system. The transfer-clock pulses are connected to the AND gates B_1 , B_2 , A_3 , and A_4 . The dump-clock pulses are connected to A_1 , A_2 , B_3 , and B_4 . The output of OR gates D_1 and D_2 are connected to Buffer B's clock pulse input, pin 6, and the output of OR gates D_3 and D_4 are connected to Buffer C's clock pulse input, pin 6. Figure 21A shows that a logical "1" at K_A will enable all "A" AND gates routing the dump-clock pulses to Buffer B and the transfer-clock pulses to Buffer C. A logical "1" at K_B will enable all "B" AND gates, routing the dump-clock pulses to Buffer C and the transfer-clock pulses to Buffer B.

Pins 12 and 13 of Card 2 are connected to pin 3 of each buffer. A logical "1" at pin 12 selects Buffer B to receive new data and logical "1" at pin 13 selects Buffer C.

Combining the action of the Register-Select signal on U25 and Buffers B and C, it can be noted that when a logical "1" is at pin 12, U25 selects Buffer B to receive the transfer-clock pulses and Buffer C to receive the dump-clock pulses. The logical "1" also appears at the Select Input, pin 3 of Buffer 1, enabling Buffer B to accept new data. A logical "1" at pin 13 reverses the roles of Buffers B and C.

Figure 21B shows the configuration of either U26 or U27. Since their operation is identical, only one of the gates will be shown and discussed. These gates are connected in such a manner that a logical "1" at pin 12 enables the "A" AND gates and the outputs of Buffer B are routed to pins 14 through 21 of Card 2. When a logic "1" exists at pin 13, the "B" AND gates are enabled and the outputs of Buffer C are routed to the output pins (pins 14 through 21) of Card 2.

A



B

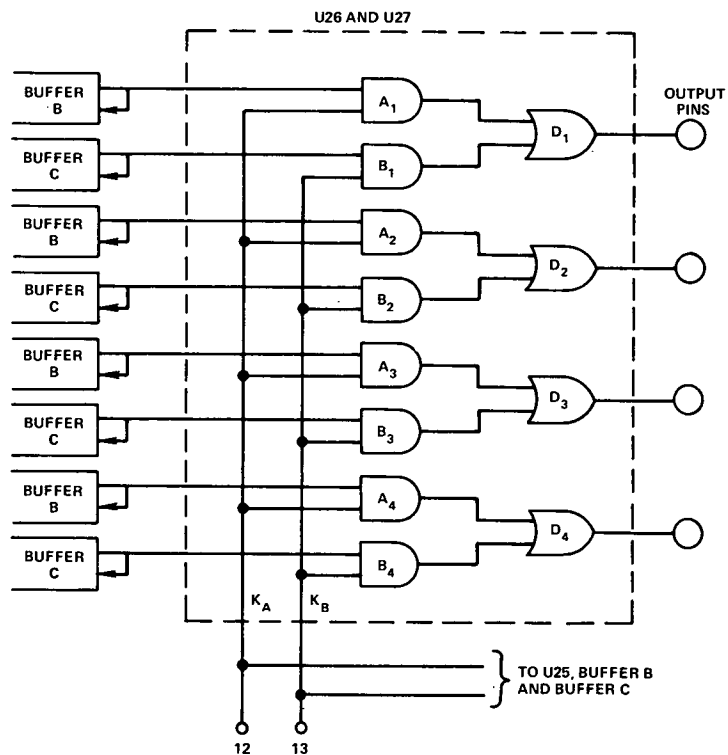


Figure 21. Memory Buffer Gate Configurations

P. SELECT

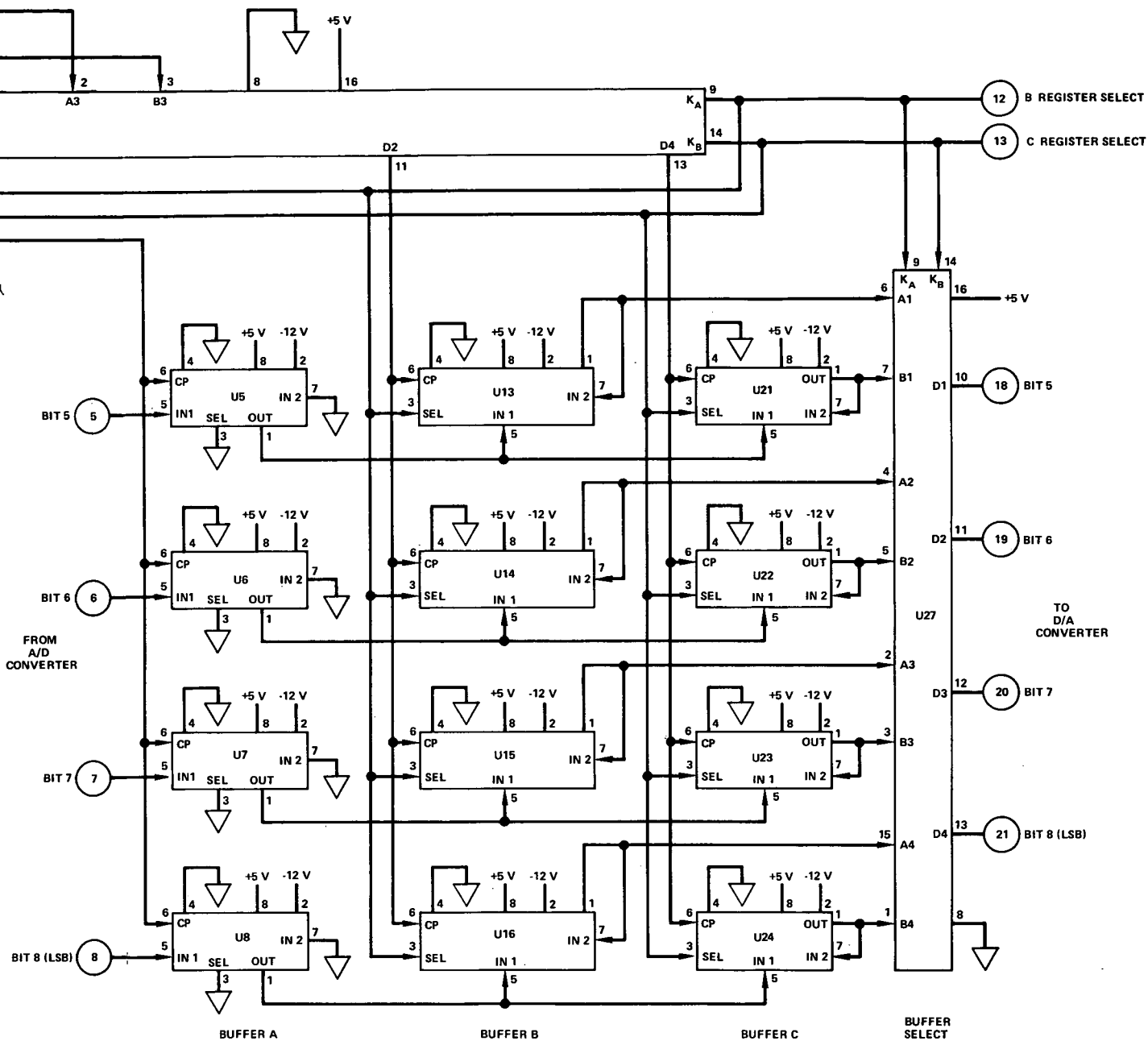


Figure 22. Memory Buffer Card (Card 2), Schematic Diagram

Timing and Clock Pulse Generator Card (Card 1)

Figure 25 is a schematic diagram of Card 1.

The Timing and Clock Pulse Generator Card (Card 1) generates the timing signals and clock pulses through the use of the following circuits:

1. Load oscillator
2. Transfer oscillator
3. Dump oscillator
4. Time-base generator
5. Buffer-toggling control.

The Load Oscillator is used to generate a pulse train which initiates each sample of the input video by the Analog/Digital (A/D) converter portion of Card 3 and simultaneously shifts Buffer A one stage per input pulse.

The Transfer Oscillator is used to generate a pulse train which shifts the contents of Buffer A to either Buffer B or C whichever is selected for the Standby-to-Receive Mode. Each of the two buffers, Buffer A and the receiving buffer selected, either B or C, is shifted one stage per input pulse.

The Dump Oscillator is used to generate a pulse train which shifts one of the selected buffers, (B or C), to provide output data to the digital/analog (D/A) converter portion of Card 3. The output buffer is shifted one stage per input pulse.

The Buffer-Toggling control circuits ensure that the transfer of output responsibility of Buffer B to Buffer C, or vice versa, is not permitted either while the output buffer is in the process of providing its data or while data are being transferred from Buffer A to Buffer B or C, whichever is in the Standby-to-Receive state.

Card 1 operates in two modes, the normal mode (nonlinearized) and linear correction mode (linearized). In the nonlinearized mode, the APT Digital Scan Converter presents distorted data to the Display Monitor, correcting the scan time from the satellite's radiometer 48-rpm format to the scan time of the Display Monitor. This correction will hereafter be referred to as Time-Based Correction. In this mode the operator may select a small sector of the area of earth's surface being transmitted by the satellite and amplify it to cover the full width of the Display Monitor. This is accomplished by adjusting the front panel's LOAD-START control which will determine where the scan will begin and by adjusting the load oscillator frequency to coincide with the swath of earth's surface to be studied.

In the linearized mode, the Load-Start time and load clock frequencies are preset and will present 35 percent (2,270 miles) of the distorted earth's surface transmitted by the satellite. Both the Time-Base Correction of the nonlinearized mode and Panoramic Distortion Correction are performed in this mode.

Brief Circuit Description

The operation of Card 1 functions in exactly the same manner for both linearized and non-linearized modes with the exception of replacing the pulse train generated by its Load Oscillator with the pulse train generated by the Load Oscillator of Card 5. Therefore, in the following discussion, distinction will be made as to the mode of operation only when applicable.

The primary sync signal is received from Card 6. A secondary sync signal is generated which, in the nonlinearized mode, is delayed by a time determined by the Front Panel LOAD START control. This control determines at which point in the transmitted scan the sampling begins. In the linearized mode this delay is fixed and is coincident and compatible with the slope at the beginning of the correction curve generated in Card 5.

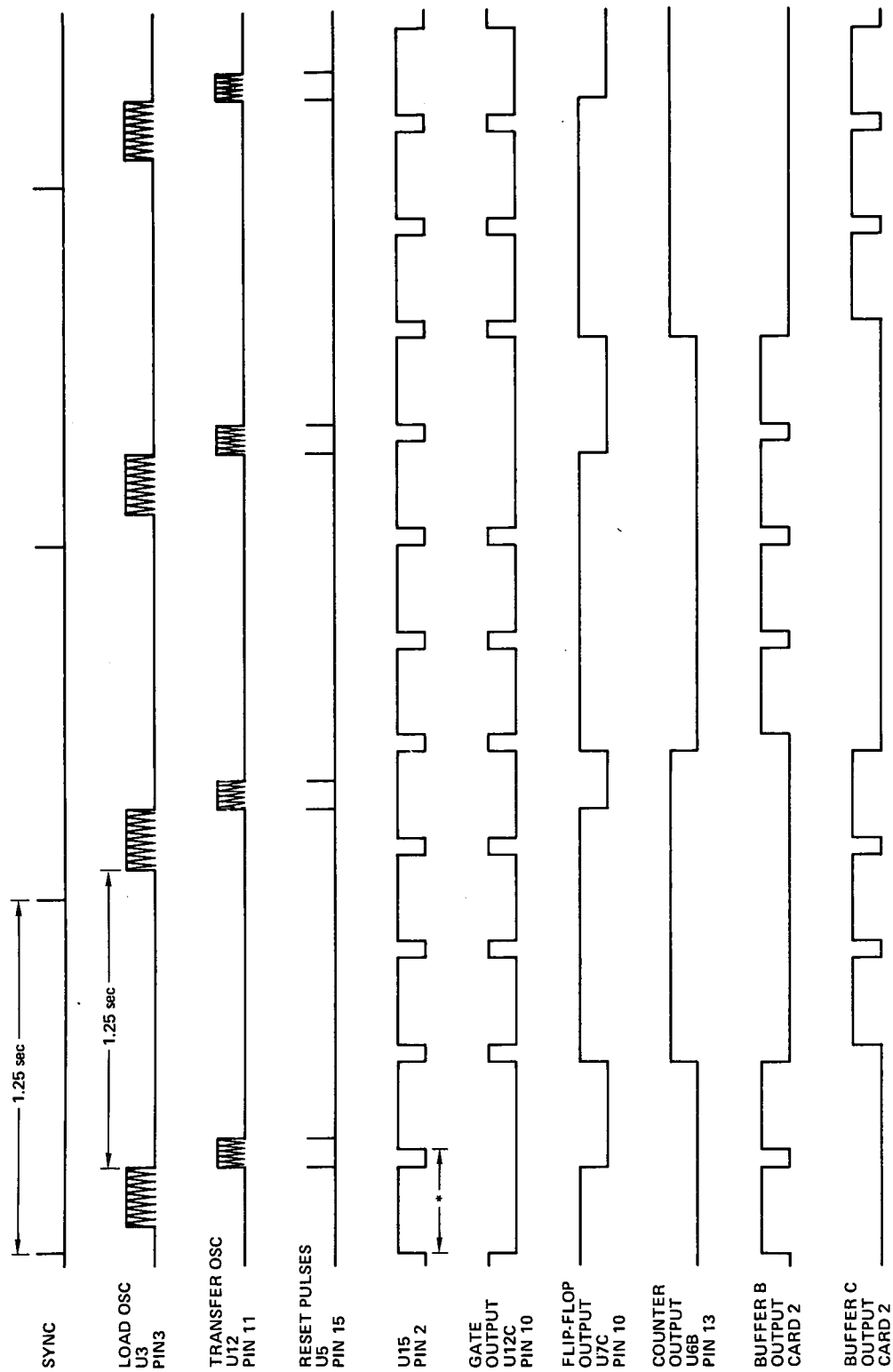
This delay is accomplished by using a one-shot multivibrator. The trailing edge of the one shot multivibrator sets the Flip-Flop S/RA, U2C and U2D, which enables Load Oscillator U3. The output of S/RA is sent to the Analog/Digital (A/D) portion of Card 3. The load pulses are counted by the counter U5 and when a count of 1024 pulses is reached, a Reset Pulse is generated (figure 23) which disables the Load Oscillator.

The Reset Pulse initiates the enabling of the Transfer Oscillators U7A and U7B and readies the Buffer Toggling circuits. The output of the Transfer Oscillator also is counted and when a count of 1024 pulses is reached (meaning the transfer of new data to the Standby Buffer is complete), a second Reset Pulse is generated which disables the Transfer Oscillator, thus satisfying one of the two conditions required for Buffer Toggling. (These two conditions are discussed in more detail later in the text.) Both the Load and Transfer Oscillators now stand idle until a new sync pulse arrives from Card 6.

The Time Base Generator is simply a countdown circuit which generates a pulse train whose frequency is selected from 96 ppm, 120 ppm, or 240 ppm. This pulse train is the reference to which the scan of the Display Monitor is synchronized. That is, the pulse out of the Time Base Generator must be coincident with the beginning of each scan of the display. Since this pulse represents the beginning of each scan of the Display Monitor, it is used to enable Dump Oscillator U8. The pulse train out of Dump Oscillator U8 is counted and when a count of 1024 pulses is reached, the Dump Oscillator is disabled and waits for the next time-base pulse.

Detailed Circuit Description

The primary sync pulse is brought into Card 1 through pin 1. Capacitor C1 removes any d.c. component from the incoming signal. Resistors R1 and R2, diodes CR1 and CR2 shape and limit the input of U2A, pin 1, from 0 to +5 volts. U1 is a One-Shot Multivibrator whose pulse width is determined by R104, R3 and C3 in the linearized mode. The pulse width is variable in the nonlinear mode, enabling the Scan Converter Operator to begin sampling the incoming video from pre-earth to post-earth. In the linearized mode, the sampling begins



*THIS PERIOD WILL BE: 625 ms FOR 96 RPM OPERATION
 500 ms FOR 120 RPM OPERATION
 250 ms FOR 240 RPM OPERATION

Figure 23. Timing Diagram (Reset Pulse)

precisely 18.89 ms after sensing earth's edge at the beginning of the sweep. This pulse is inverted through U2B and routed to Card 5 through pin 3 of Card 1 which initiates the linearization function of Card 5. It is also provided through C4 to R5 and to CR3 of Card 1 which sets Flip/Flop S/RA.

By setting S/RA, pin 10 of U2C goes to a logical "0" state, disabling the Dump Oscillator of Card 5. Pin 11 of U2D goes to a logical "1" state, thus enabling Load Oscillator U3. The output of U3 goes through pin 5 of Card 1 to the NORMAL/LIN correction switch S102, on the Front Panel. Switch S102 selects either load pulses from Card 5 or the load pulses from Card 1. The load pulses enter Card 1 through pin 6 and exit through pin 11 to the Front Panel's test point, J107, the Analog/Digital (A/D) portion of Card 3, and the buffer of Card 2. Additionally, load pulses are provided as input at pin 2 of U13 through decoupling capacitor C16. U13 is a One-Shot Multivibrator which shapes and gives a uniform width to the load pulses coming from U3 of Card 5. Resistor R29 and capacitor C28 determine that width.

U7B and U7A are NOR gates configured to form the Transfer Oscillator. The frequency is determined by R10 and C8. The function of R11 is for protection of the Input of U7B. Because the input impedance of U7B, pin 6, is so high, R11 has no influence on the frequency of the oscillator and therefore is not critical. The oscillator runs at approximately 500 kHz. The output of U12D, pin 11, and U13, pin 3, is the inputs of NOR gate U4C. When Load Oscillator U3 is disabled, pin 3 of U13 is low; and when the Transfer Oscillator is disabled, pin 11 of U12D is low, and since only one oscillator operates at a time, U4C acts as an OR gate. Therefore, the output of U4C will carry both load or transfer pulses. The output of U4C is inverted by U4D and this output is routed to the Buffer gates of Card 2. The output of U4D also feeds the input to the 1024 bit counter, U5.

The count of 1024 is sensed at pin 15 of U5 and is applied to pin 11 of U5 through R9 and C7 which resets the counter. Resistor R9 and capacitor C7 determine the width of the pulse at pin 15. This Reset Pulse resets Flip-Flop S/RA, thus disabling Load Oscillator U3, and Load Oscillator U5, on Card 5. This Reset Pulse also toggles counter U6A. The output of U6A is a.c. coupled to one input of S/RB through C9 and shaping components R12 and CR4 to pin 8 of U7C. C9, R12, and CR4 allow only narrow positive going pulses to reach pin 8 of U7C. These pulses set pin 10 of U7C low or at logical "0", thus enabling Transfer Oscillator U7.

The 2.4 kHz clock-pulses enter Card 1 through pin 35. Transistor Q1 is a pulse-shaping stage whose output feeds the clock input to the countdown circuit U16, pin 10. The output of U16 is fed to NAND gates U18, U19 and U20 which detects the binary code 10110111000 (binary 1500), binary code 10010110000 (binary 1200) and binary code 01001011000 (binary 600) respectively. The outputs of the gates go to pins 27, 28, and 29 of Card 1 and to switch S103B on the Front Panel. Switch S103B selects the gate, producing a time base compatible with the Display Monitor. The output of the selected gate goes back into Card 1 through pin 30 to pin 5 of U12B where it is inverted and routed through R21 and C18 to

the reset pin 11 of U16. The length of the pulse at pin 4 of U12B is determined by R21 and C18. This pulse is applied at pin 4 to reset Flip-Flop U15. Resetting U15 puts pin 2 of U15 to a logical "1" which enables Dump Oscillator U8. The output of U8, pin 3, is fed through decoupling capacitor C19 to U14, pin 2. U14 is a One-Shot Multivibrator which shapes and sizes the pulse and routes it to the Dumping Buffer of Card 2. The width of the pulse of U14 is determined by R31 and C21.

The period of the sync signal (primary and/or secondary sync pulses) and the period of the Time-Base Generator U16 are not equal. The period of the sync signal is equal to 1.25 sec and the period of the Time-Base Generator is 625 ms when 96 rpm is selected; 500 ms when 120 rpm is selected; and 250 ms when 240 rpm is selected (figure 24).

Therefore, data will be shifting into and out of Buffer A at a frequency that is totally independent of the operation of the Dumping Buffers whose dump period is controlled by the Time Base Generator.

To resolve this problem, an extra buffer is provided to operate in a Standby-to-Receive data mode while another buffer is dumping data to the Display Monitor. Once the buffer in the Standby-to-Receive data mode has received a complete line of new data, it must now assume the role of the Dumping Buffer and the buffer most recently dumping assumes the role of the Standby-to-Receive Buffer.

This changeover cannot occur during the time that either the Output Buffer is dumping or the Standby-to-Receive Buffer is receiving data. Therefore, the logic of stages U12C, U7D, U7C, and C9, R12 and CR4 must require that if, and only if, the two following conditions are met, the buffer responsibility of Buffer B and Buffer C be switched.

1. The Dump Oscillator is inoperative.
2. The Transfer Oscillator is inoperative.

U6B is the Flip-Flop that toggles Buffer B and Buffer C of Card 2. The output of U6B toggles only when a positive going edge of a Step Function or Pulse-Input signal is applied to pin 11 of U6B. This occurs only when S/RB is first set and then reset. S/RB is set by applying a positive voltage at pin 8 of U7C and zero potential at pin 13 of U7D. This condition brings pin 10 of U7C to a logical "0". S/RB is reset by applying a positive voltage at pin 13 of U7D and zero voltage at pin 8 of U7C. This conditions brings pin 10 of U7C to a logical "1". Thus, a set followed by a reset generates a toggle of U6B.

Figure 24 (Sheets 1 and 2 of 2) is a Timing Diagram showing the timing interrelationship between the Dump Oscillator control, the Transfer Oscillator and toggling Flip-Flop U6B. U6B occurs only when the Dump- and Transfer-Oscillators are disabled.

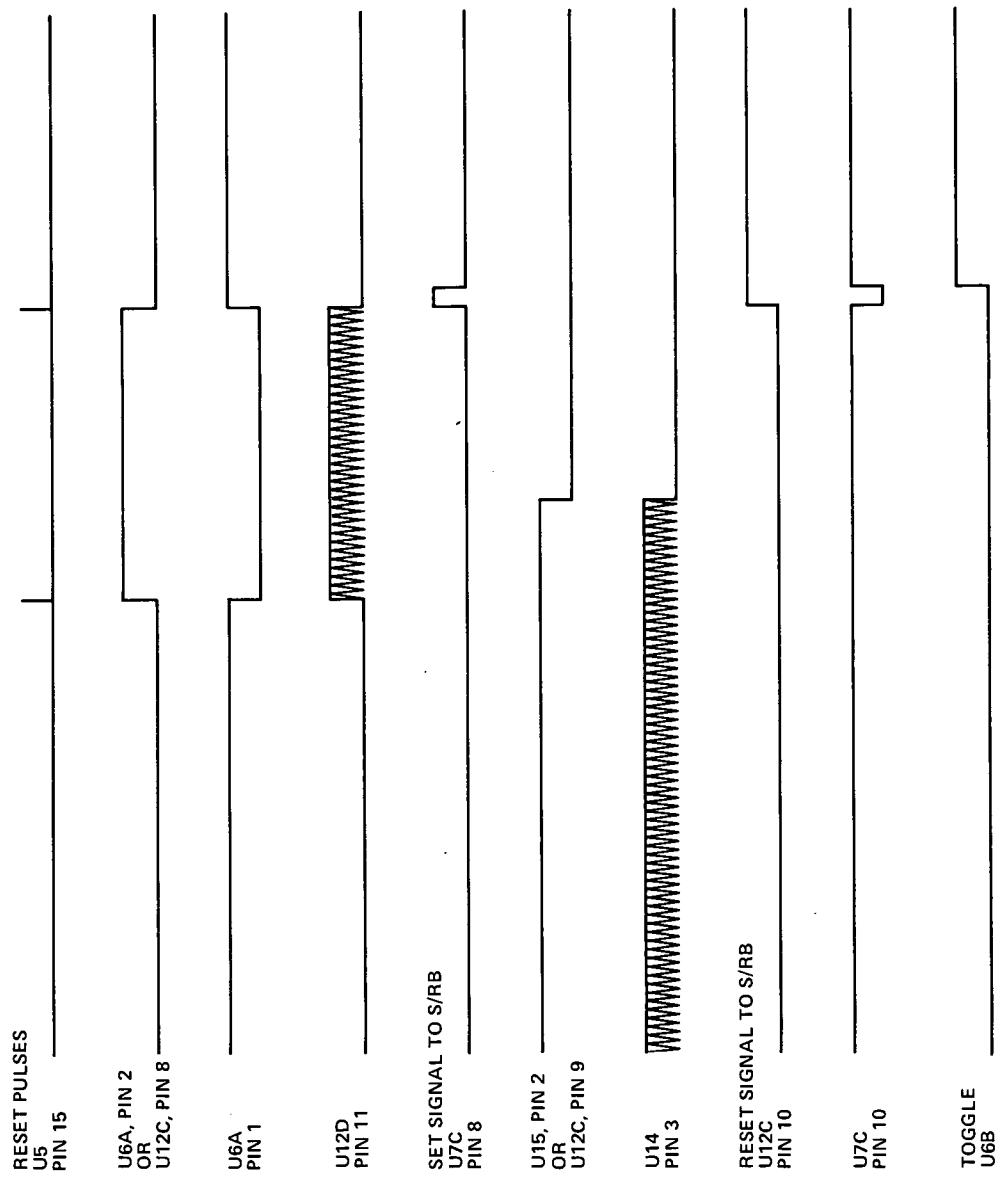


Figure 24. Timing Diagrams for Dump Oscillator Control, Transfer Oscillator, and Toggling Flip-Flop Amplifier U6B (Sheet 1 of 2)

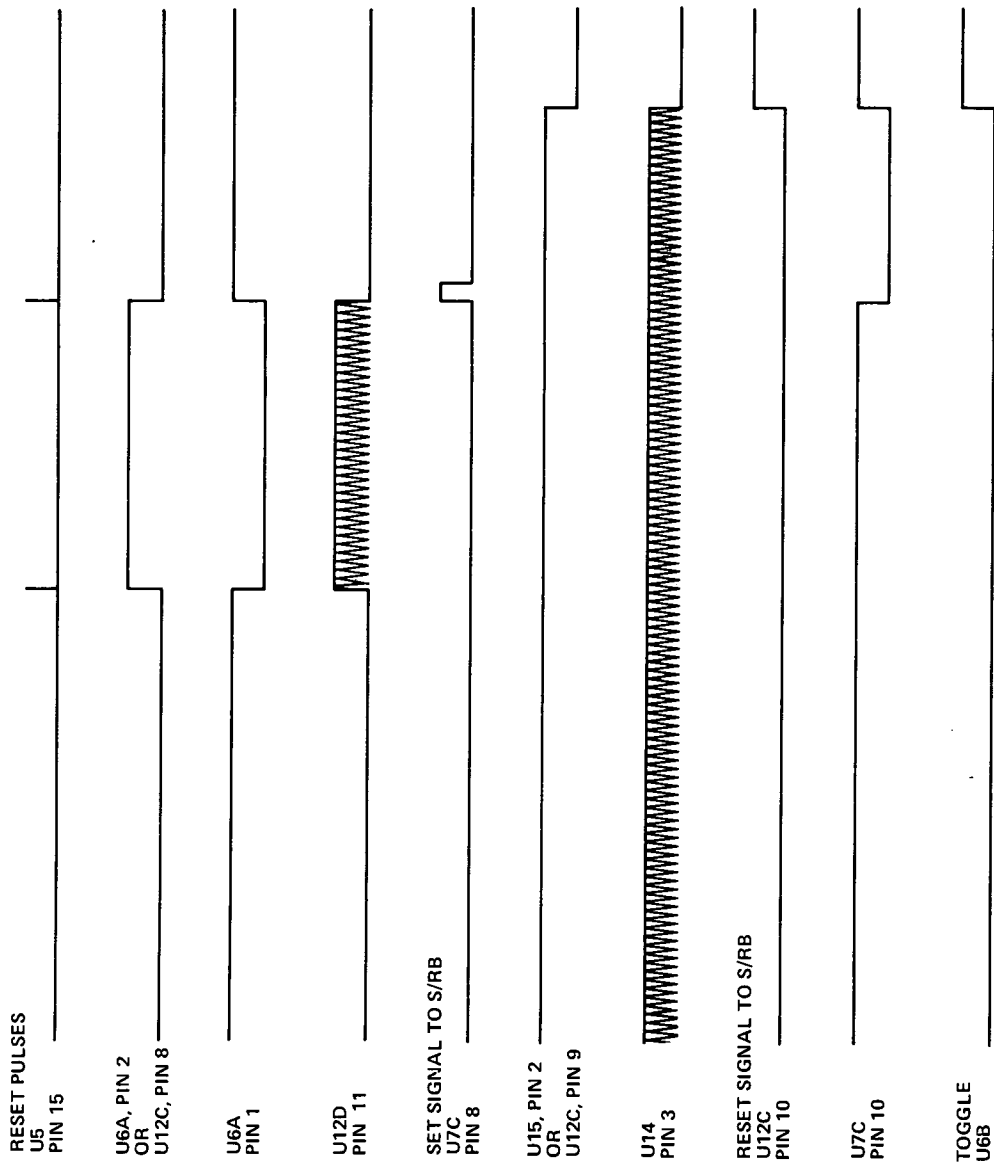
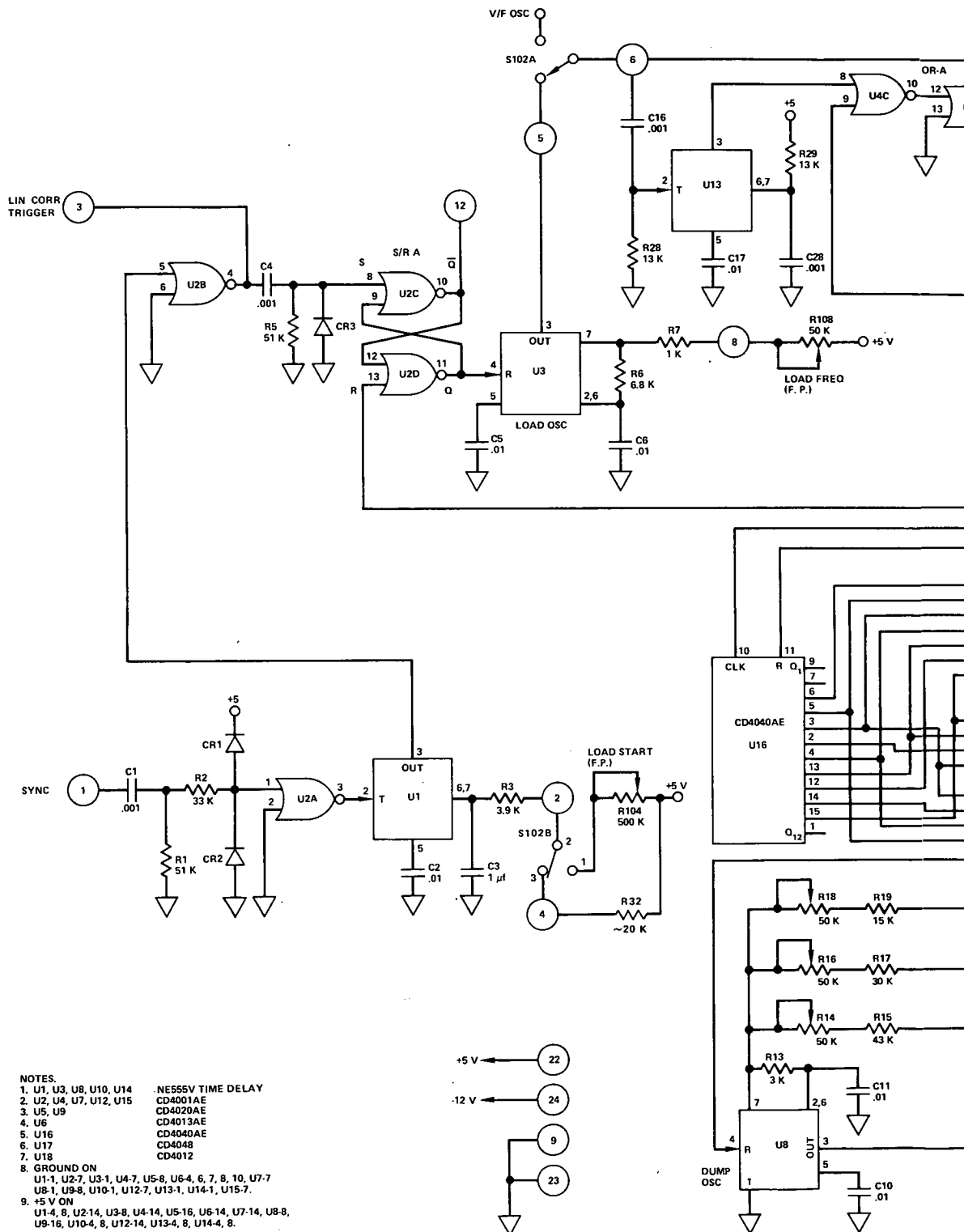


Figure 24. Timing Diagrams for Dump Oscillator Control, Transfer Oscillator, and Toggling Flip-Flop Amplifier U6B (Sheet 2 of 2)



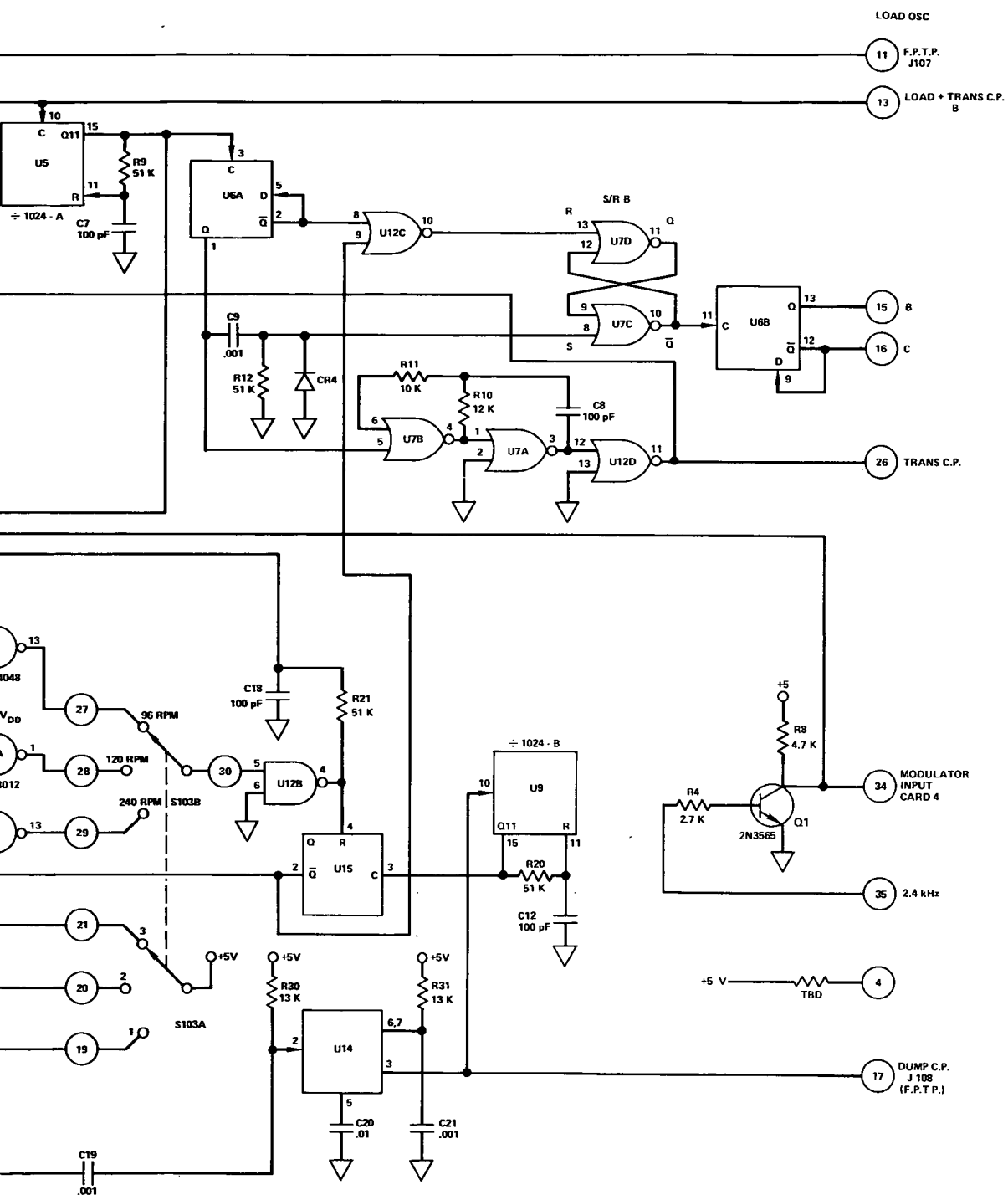


Figure 25. Timing and Clock Pulse Generator Card (Card 1), Schematic Diagram

CONSTRUCTING THE APT DIGITAL SCAN CONVERTER

Construction of the APT Digital Scan Converter can be accomplished by carefully reading and studying the schematics, wiring diagram, and parts list provided in this document. Because it is anticipated that most supplies will be purchased locally, at each station, the parameters of the major components are supplied, along with a suggested source. The level of information provided is based on the assumption that the builder is competent in the field of electronics and has sufficient test equipment. (See Appendix C for a list of specific test equipment required.)

The physical arrangement of the unit may be varied to adapt to the local ground station and the availability of mechanical components. Careful consideration must be given to matching the input and output impedance of the converter and the ground station equipment. Major considerations are:

- Take every precaution to prevent wiring errors,
- Check each component before it is used.

Mechanical Assembly

Major components of the mechanical assembly involve the chassis, case, and front panel. The APT Digital Scan Converter built at NASA uses a 29 by 40 by 7.4 cm (10 by 17 by 3 in.) preformed chassis (with an added front panel) housed in a 28 by 28 by 46 cm (11 by 11 by 18 in.) case. Figures 26 and 27 show suggested layouts for the Front Panel and the chassis assembly, rear, respectively. Although chassis layout is at the discretion of the individual, care should be taken in the placement of power supplies with regard to heat dissipation and in relative routing of a.c. power and video signal wiring. Figure 28 shows the basic chassis layout with the Front Panel attached.

Circuit Cards

For ease of construction and maintenance the circuits used in the APT Digital Scan Converter are packaged functionally and mounted on perforated circuit cards. It is strongly recommended that pin and wire-wrap techniques be used when fabricating these cards and that good electronic packaging principles be followed in the layout of components. Figures 29 through 34 show the general layout of the six circuit cards.

The logic diagrams associated with circuit descriptions and the parts lists found in Appendix E can be used in determining component parameters and requirements. Appendix E supplies parameters for major components, along with such criteria as tolerances, wattages, and construction characteristics of miscellaneous components. Values of these miscellaneous components are found on the individual logic diagrams. Vendor part numbers and names are provided only as an aid in identification when making local purchases of equivalent components.

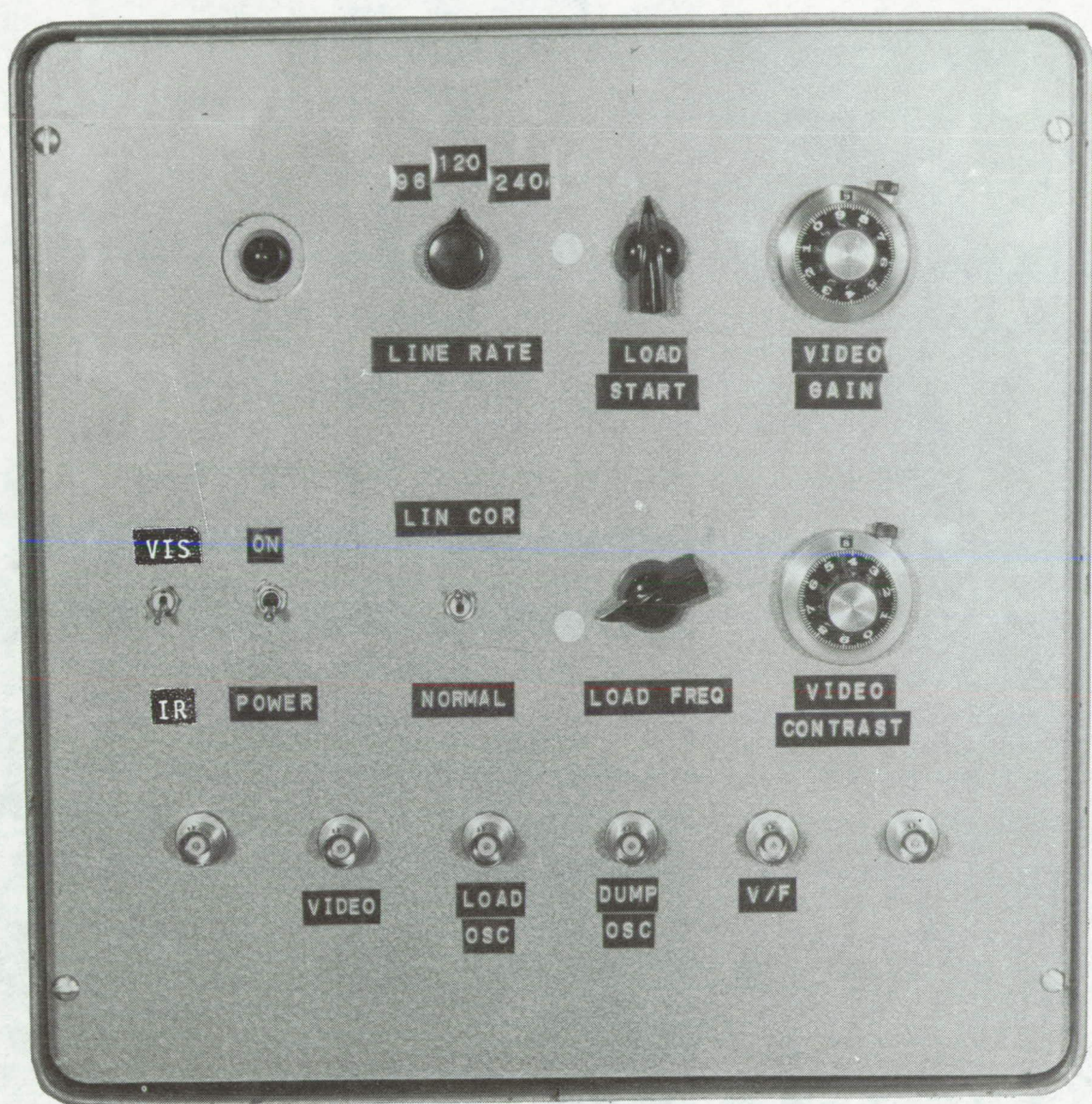


Figure 26. Front Panel

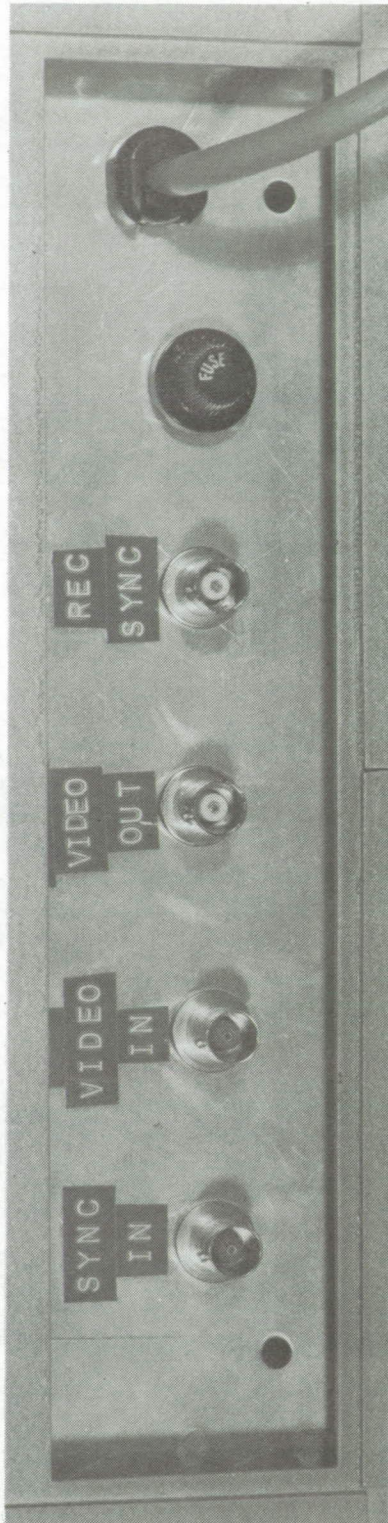


Figure 27. Chassis Assembly, Rear

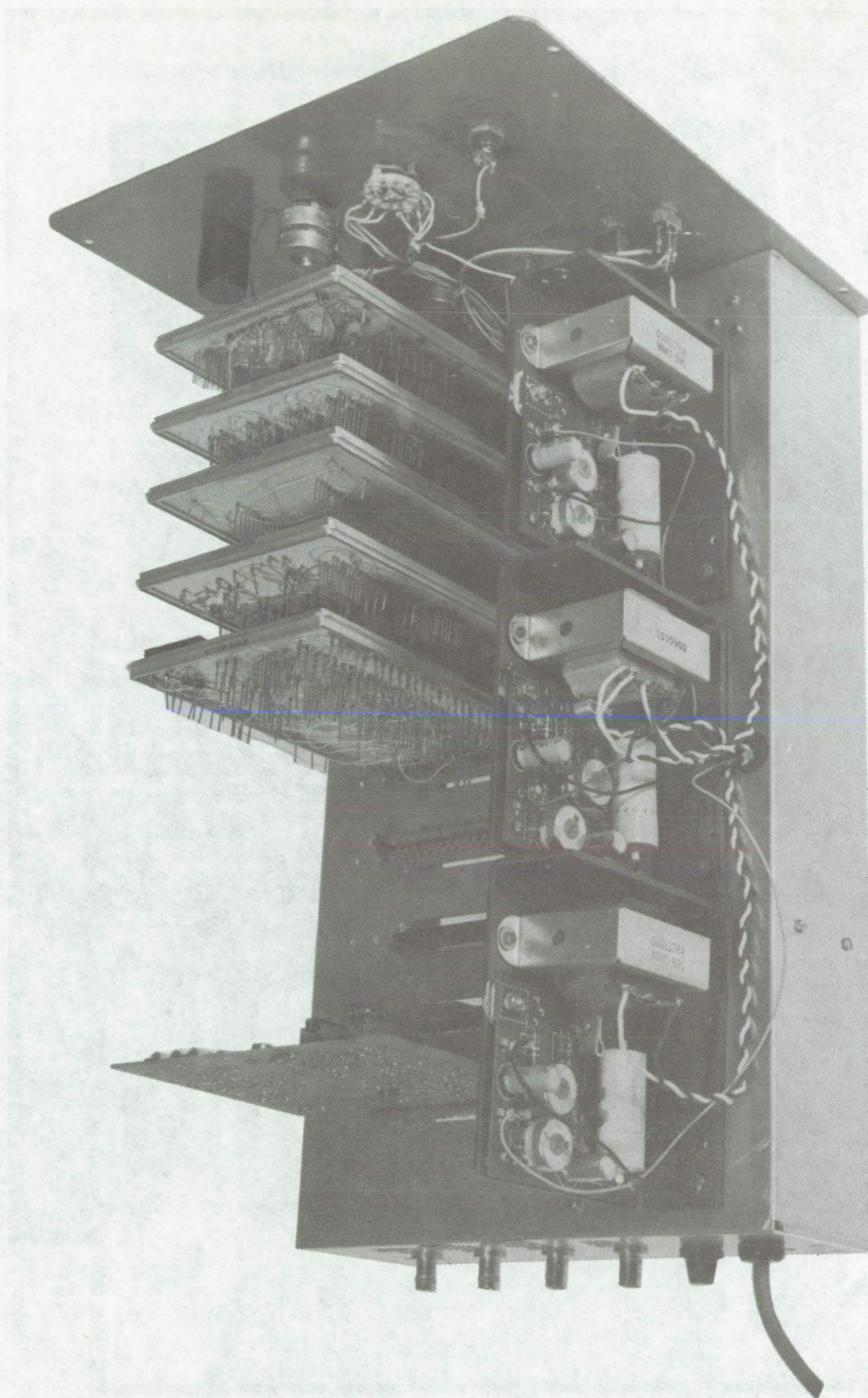


Figure 28. Chassis and Front Panel Assembly

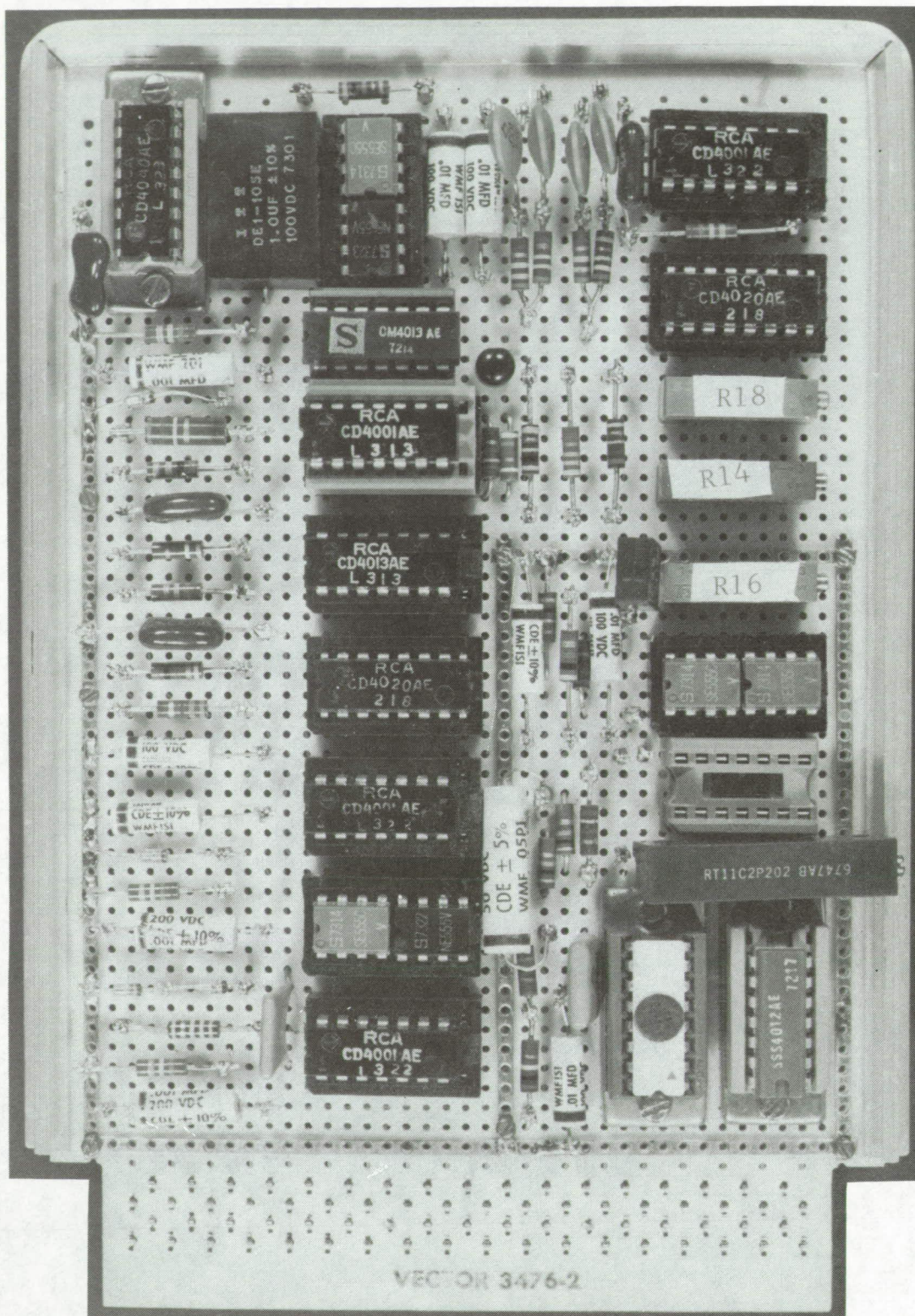


Figure 29. APT Digital Scan Adapter Control Card No. 1

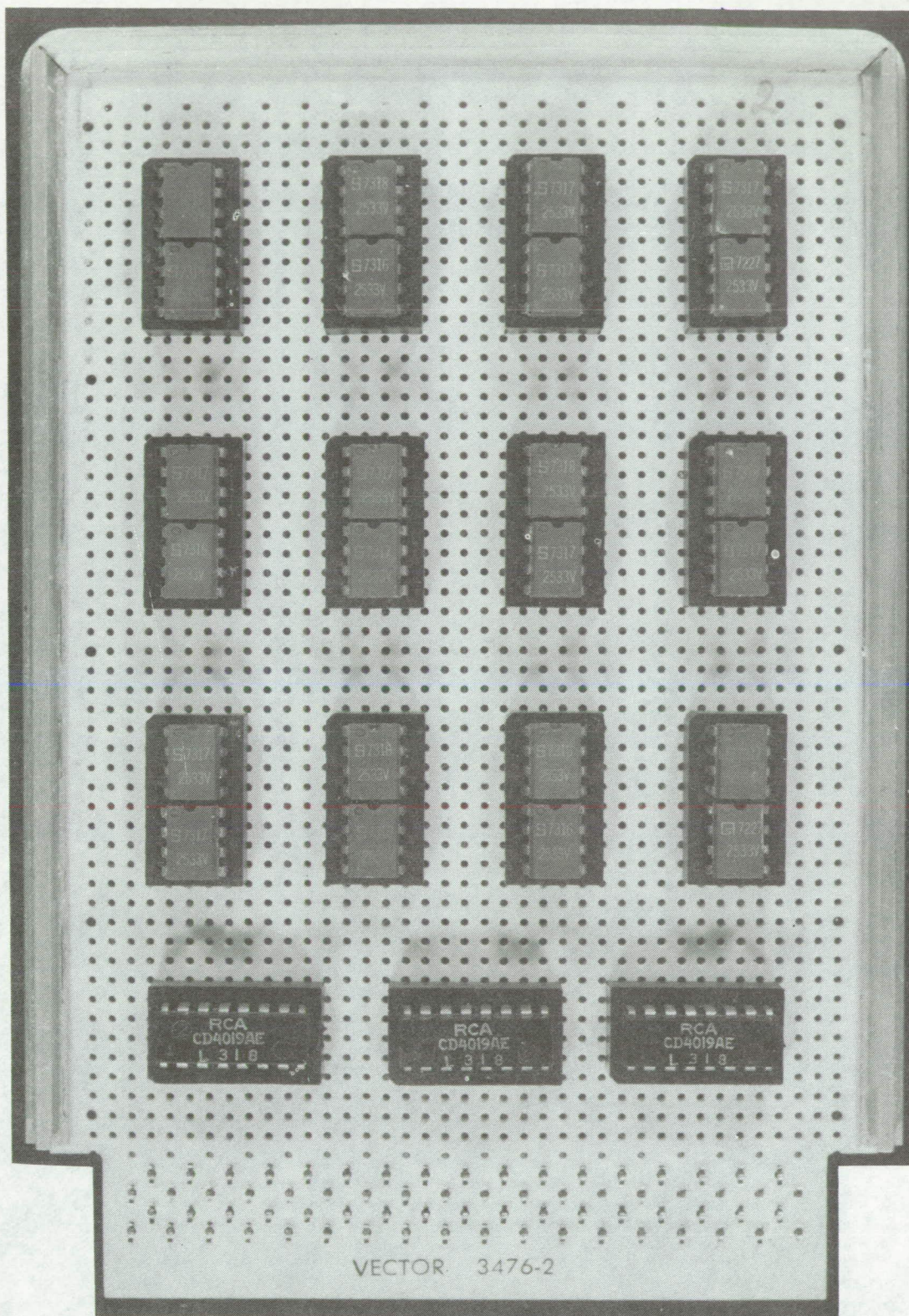


Figure 30. APT Digital Scan Adapter Control Card No. 2

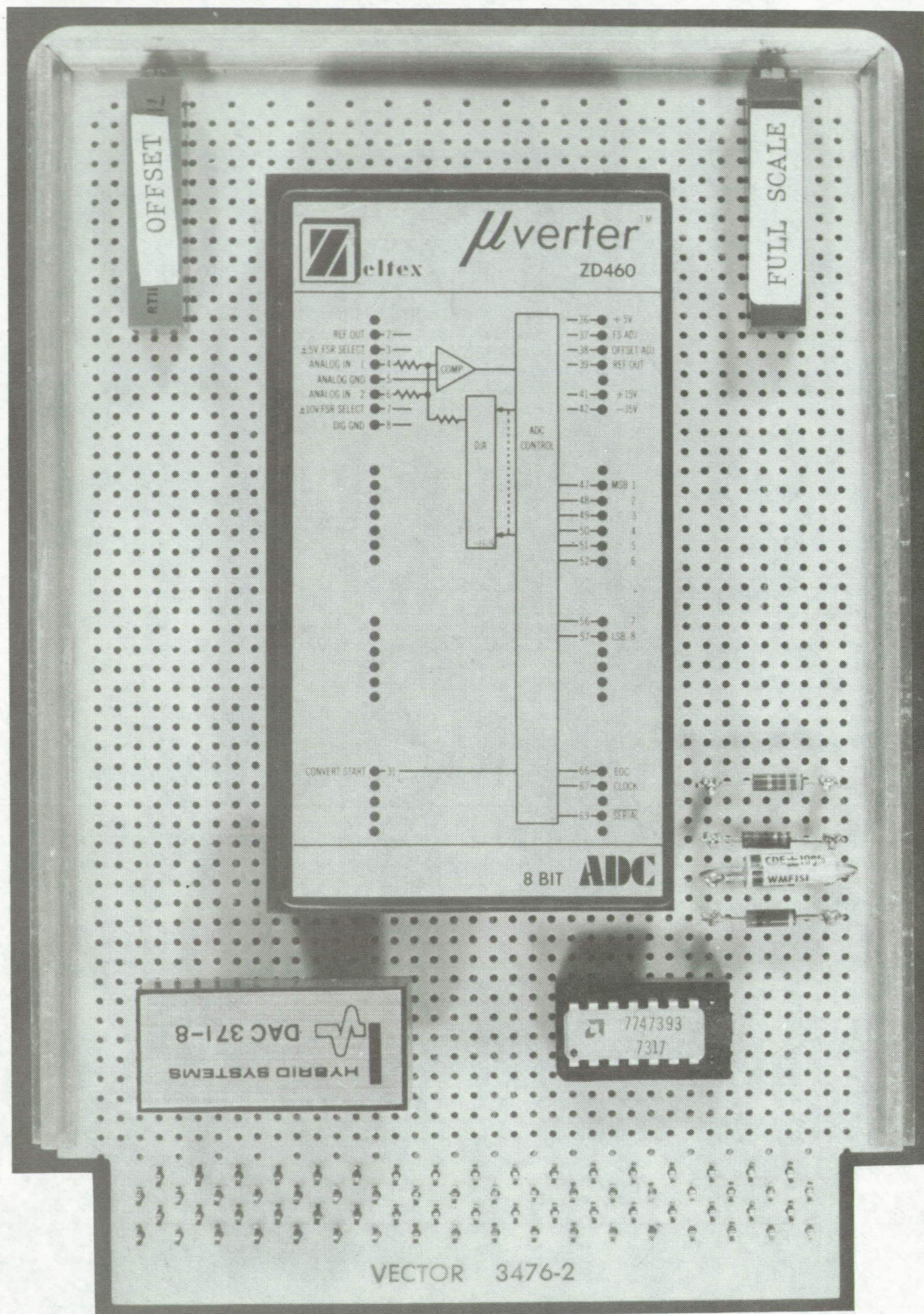


Figure 31. APT Digital Scan Adapter Control Card No. 3

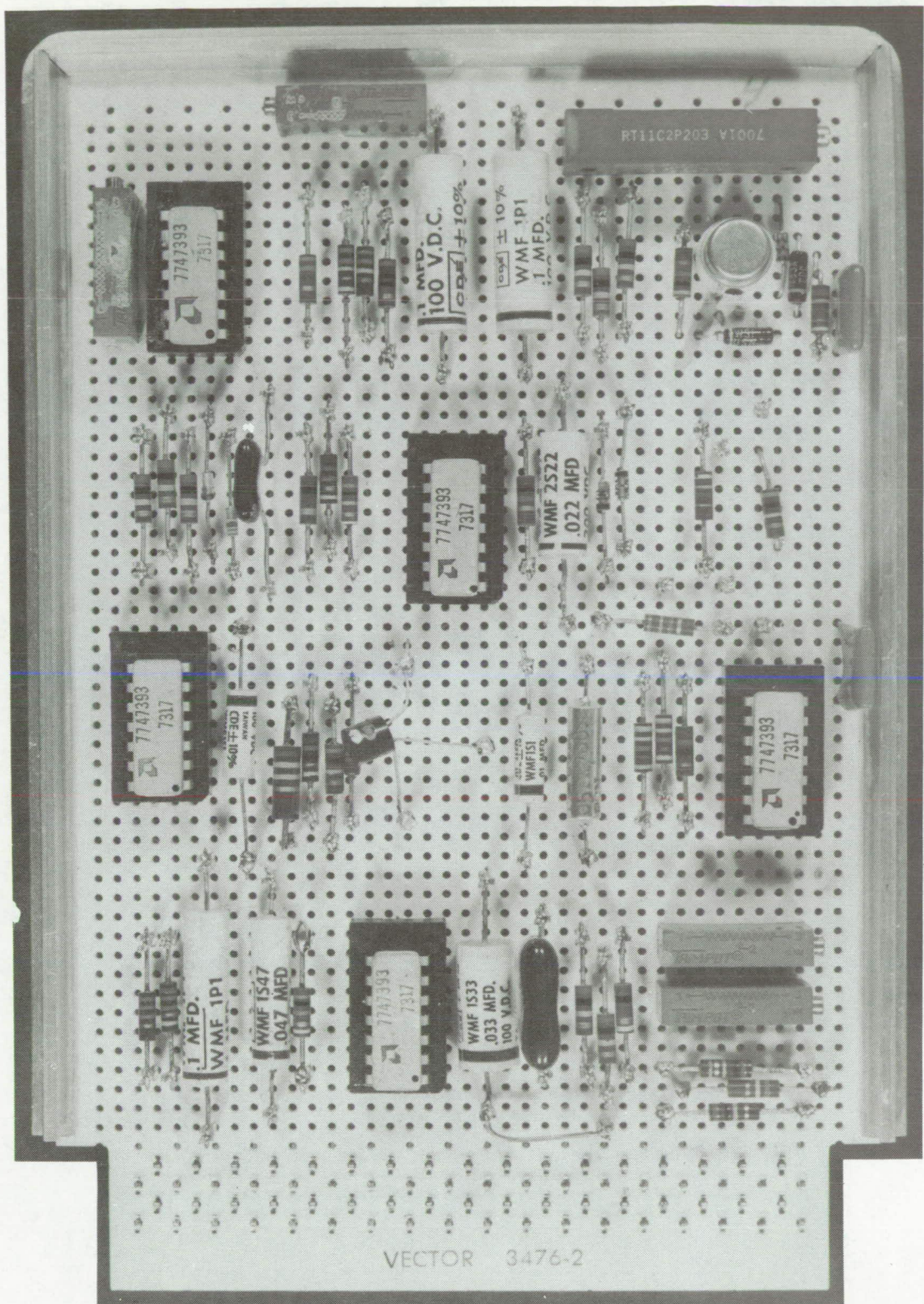


Figure 32. APT Digital Scan Adapter Control Card No. 4

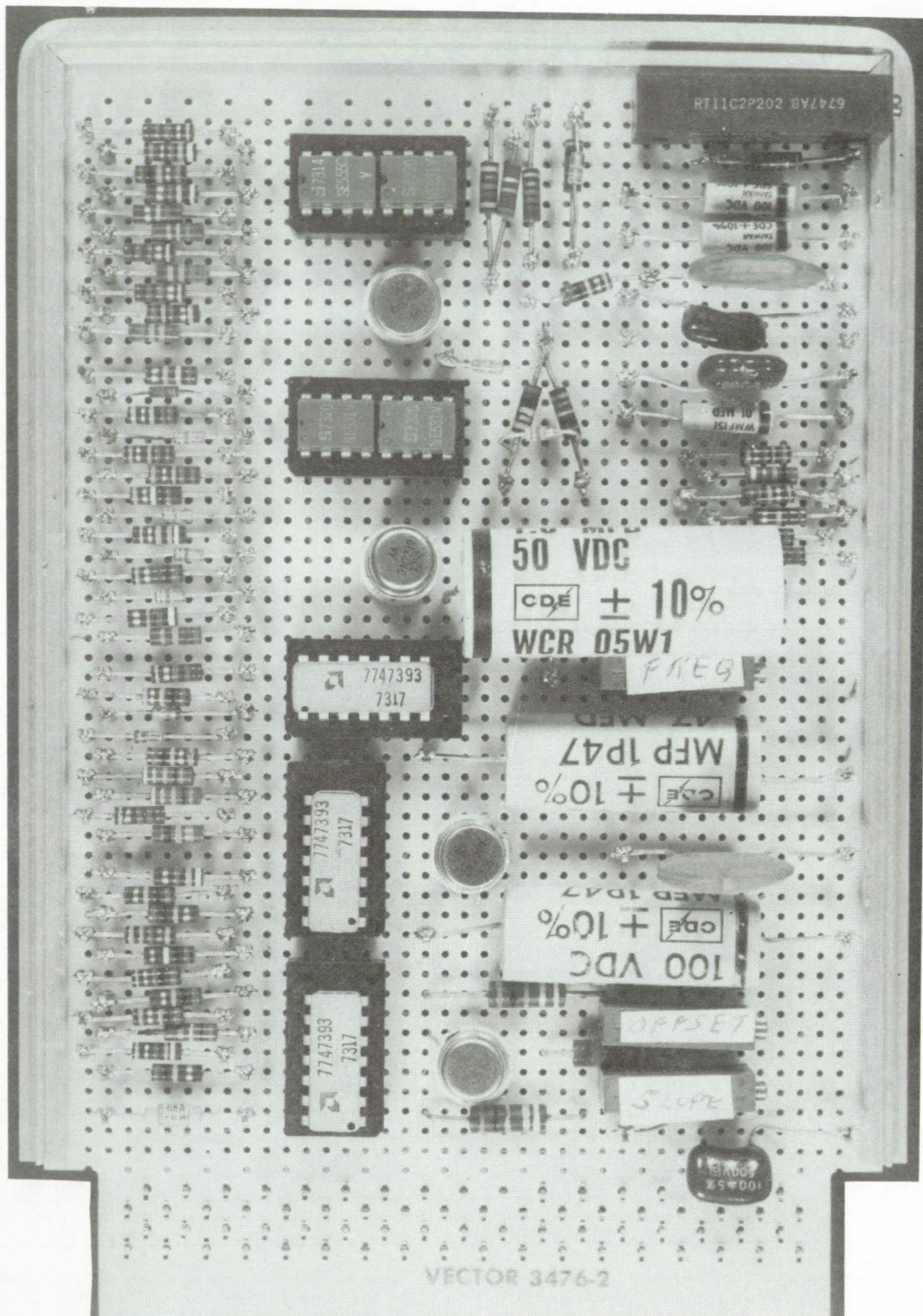


Figure 33. APT Digital Scan Adapter Control Card No. 5

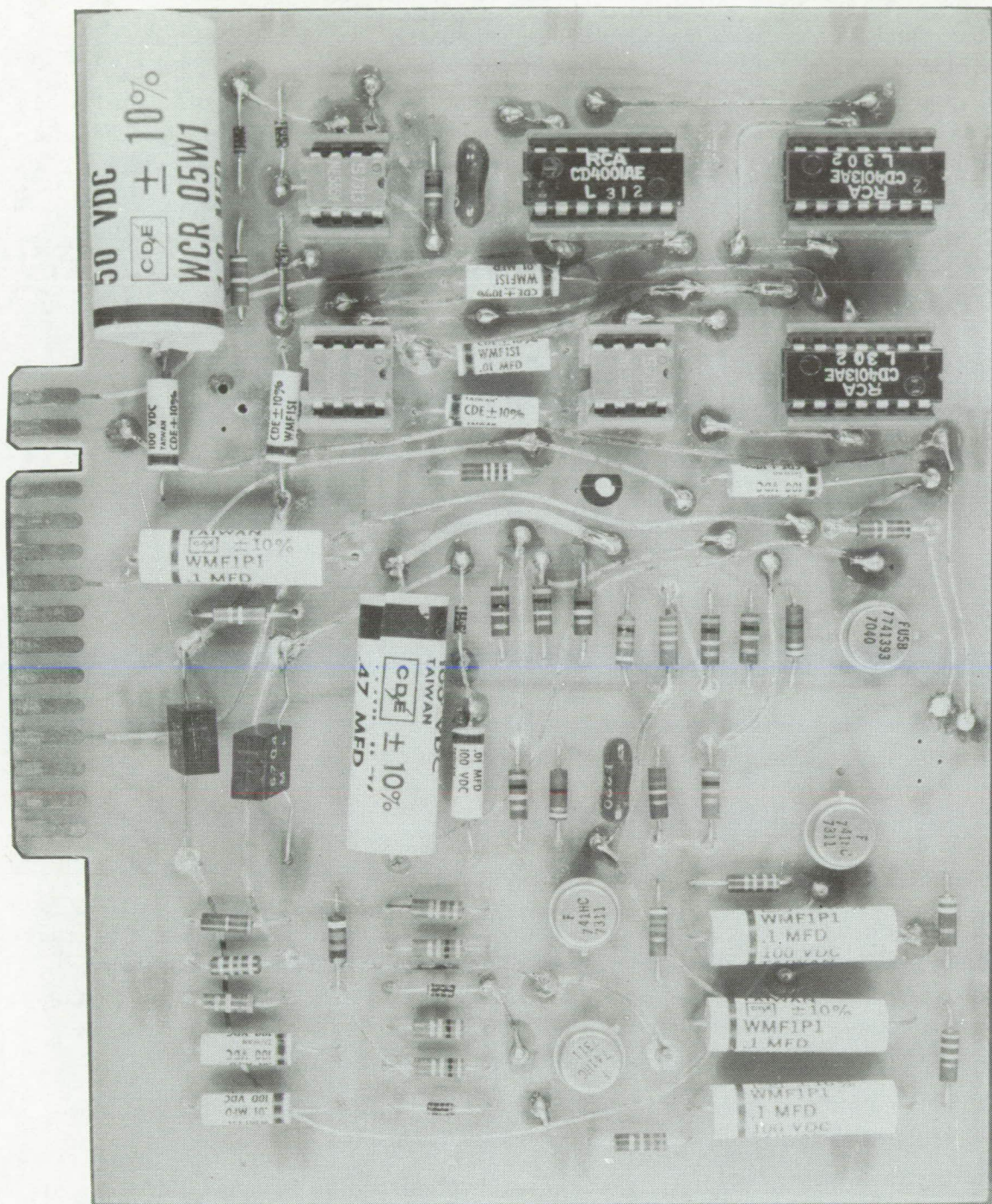


Figure 34. APT Digital Scan Adapter Control Card No. 6

Power Supplies

Three standard, commercially available power supplies are mounted on the chassis. These provide +5, +15, and -15 volts d.c. and are modular-regulated and current-limited at 1.5, 0.7, and 0.7 amperes, respectively. The -12 volts d.c. for the Memory Registers are derived from the -15-volt-d.c. power supply by using a Darlington circuit. Figure 35 is a schematic of this power supply which is hard-wired on the underside of the chassis.

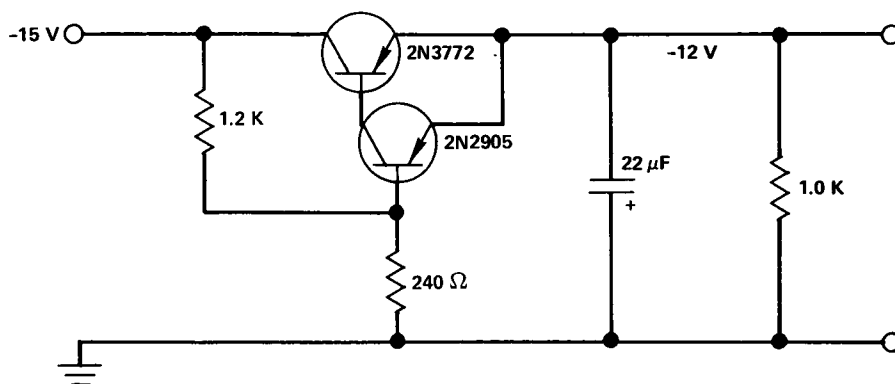


Figure 35. -12-volt-d.c. Power Supply, Schematic Diagram

Chassis Wiring

Chassis and Front Panel wiring should be accomplished in accordance with figure 36. Pairs of wires carrying a.c. power and pairs of wires carrying video signals should be twisted. All other wiring is point-to-point and should be installed using standard practices. Table 1 is a tabulation of the wiring run list.

Calibration Instructions

The circuit design techniques incorporated in the design of the APT Digital Scan Converter render the equipment relatively immune to voltage drift due to temperature and aging. Therefore, calibration of the Converter is necessary only after the construction of the Converter is complete or after equipment repair with the exception of the 2.4 kHz clock as described earlier. (Also, refer to Appendix E.)

Calibration of this equipment is accomplished on a card-by-card basis and therefore, the calibration of the cards will be discussed in ascending numerical order.

All 15-volt power supplies in the Converter should be adjusted to 15 volts \pm 5 mV prior to calibrations.

Table 1
Wiring Run List

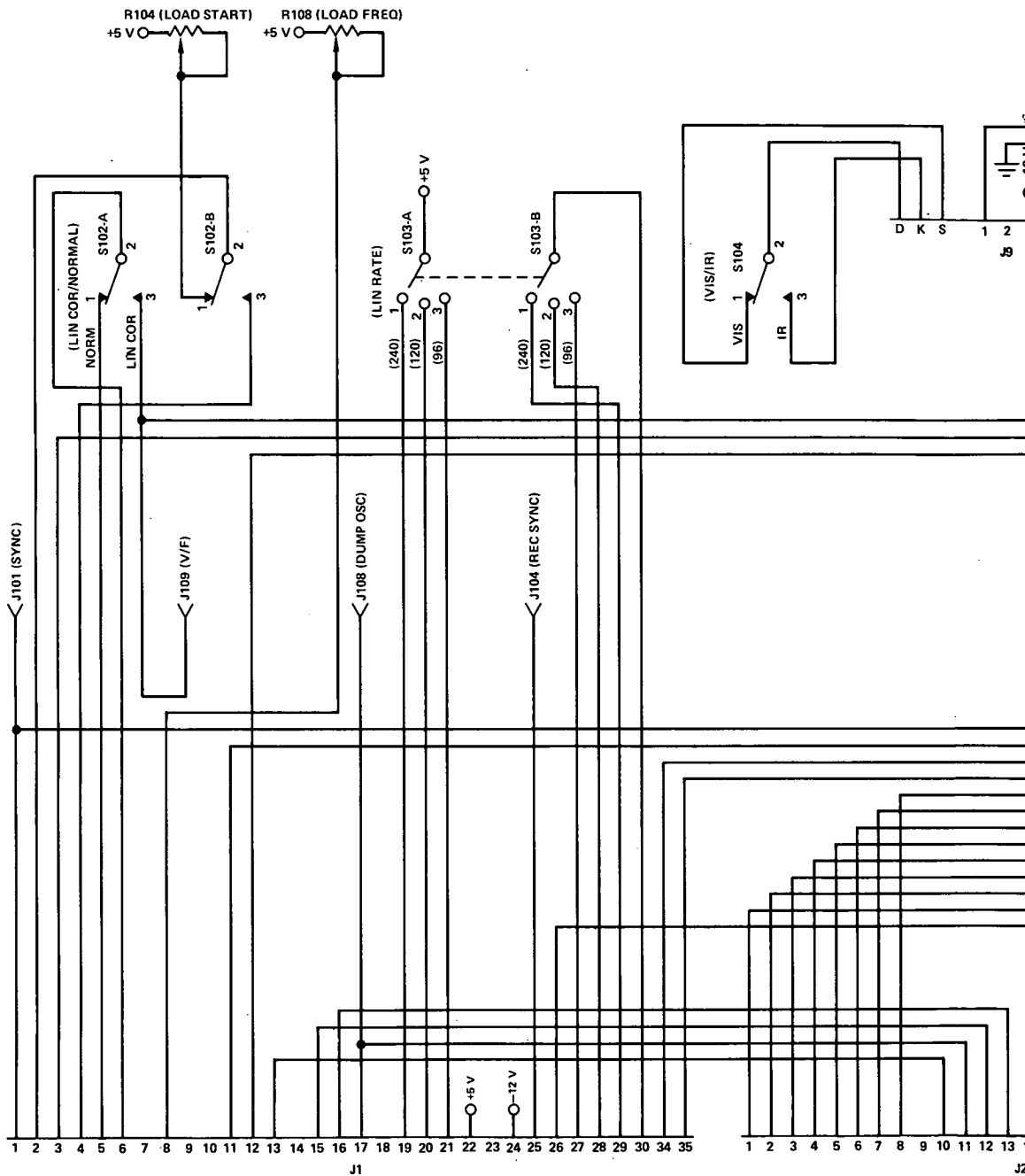
Jack Pin	J1	J2	J3	J4	J5
1	J101,J9-14, J5-1	J3-5	J106, J4-13		J9-14,J1-1,J101
2	S102B-2	J3-6			
3	J5-3	J3-7			J1-3
4	S102B-3	J3-8	J107, J1-11		
5	S102A-1	J3-10	J2-1		
6	S102A-2	J3-11	J2-2		
7		J3-12	J2-3		
8	R108-ct	J3-13	J2-4		
9	SPG	SPG	SPG	SPG	SPG
10		J1-13	J2-5	R115-ct	
11	J107, J3-4	J1-17, J108	J2-6	R115-end	
12	J5-12	J1-15	J2-7	R116-ct	J1-12
13	J2-10	J1-16	J2-8	J106, J3-1	
14		J3-14	J2-14		
15	J2-12	J3-15	J2-15		
16	J2-13,	J3-16	J2-16		
17	J108, J2-11	J3-17	J2-17		
18		J3-18	J2-18	J102, J9-1	
19	S103A-1	J3-19	J2-19		
20	S103A-2	J3-20	J2-20		J109, S102A-3
21	S103A-3	J3-21	J2-21		
22	+5 V	+5 V	+5 V	+5 V	+5 V
23	SPG	SPG	SPG	SPG	SPG
24	-12 V	-12 V	-12 V	-12 V	-12 V
25	J104		J4-32		
26	J2-26	J1-26			
27	S103B-3				
28	S103B-2				
29	S103B-1				
30	S103-B-com		+15 V	+15 V	+15 V
31			-15 V	-15 V	-15 V
32				J3-25	
33				J1-34	
34	J4-33			J103	
35	Freq. Std-6				

Table 1
Wiring Run List (continued)

From	To	Function
J101	J1-1, J5-1, J9-14	Sync
J102	J4-18, J9-1	Mod Video In
J103	J4-34	Remod Video Out
J104	J1-25	Rec. Sync
J105	Spare	
J106	J4-13, J3-1	Video to A/D
J107	J1-11, J3-4	Load Osc.
J108	J1-17, J2-11	Dump Osc.
J109	J5-20, S102A-3	V/F Osc.
J110	Spare	
R104	S102B-1-ct	Load Start
	+5 V-end	Load Start
R108	J1-8-ct	Load Freq
	+5 V-end	Load Freq
R115	J4-10-ct	Video Gain
	J4-11-end	Video Gain
R116	J4-12-ct	Black Level/Contrast
	-15 V-end	Black Level/Contrast
	+15 V-end	
S102A-1	J1-5	Linear/Normalized
S102A-2	J1-6	Linear/Normalized
S102A-3	J5-20, J109	Linear/Normalized
S102B-1	R104-ct	Linear/Normalized
S102B-2	J1-2	Linear/Normalized
S102B-3	J1-4	Linear/Normalized
S103A-1	J1-19	Line Rate
S103A-2	J1-20	Line Rate
S103A-3	J1-21	Line Rate
S103B-1	J1-29	Line Rate
S103B-2	J1-28	Line Rate
S103B-3	J1-27	Line Rate
S103A-com	+5 V	Line Rate
S103B-com	J1-30	
S104-1	J9-S	VIS/IR
S104-2	J9-D	VIS/IR
S104-3	J9-K	VIS/IR

Table 1
Wiring Run List (continued)

From	To	Function
J9-D	S104-2	
J9-K	S104-3	
J9-S	S104-1	
J9-1	J102, J4-18	
J9-3	-12 V Chassis Bus	
J9-4	GRD	
J9-5	+15 V	
J9-14	J101, J5-1, J1-1	



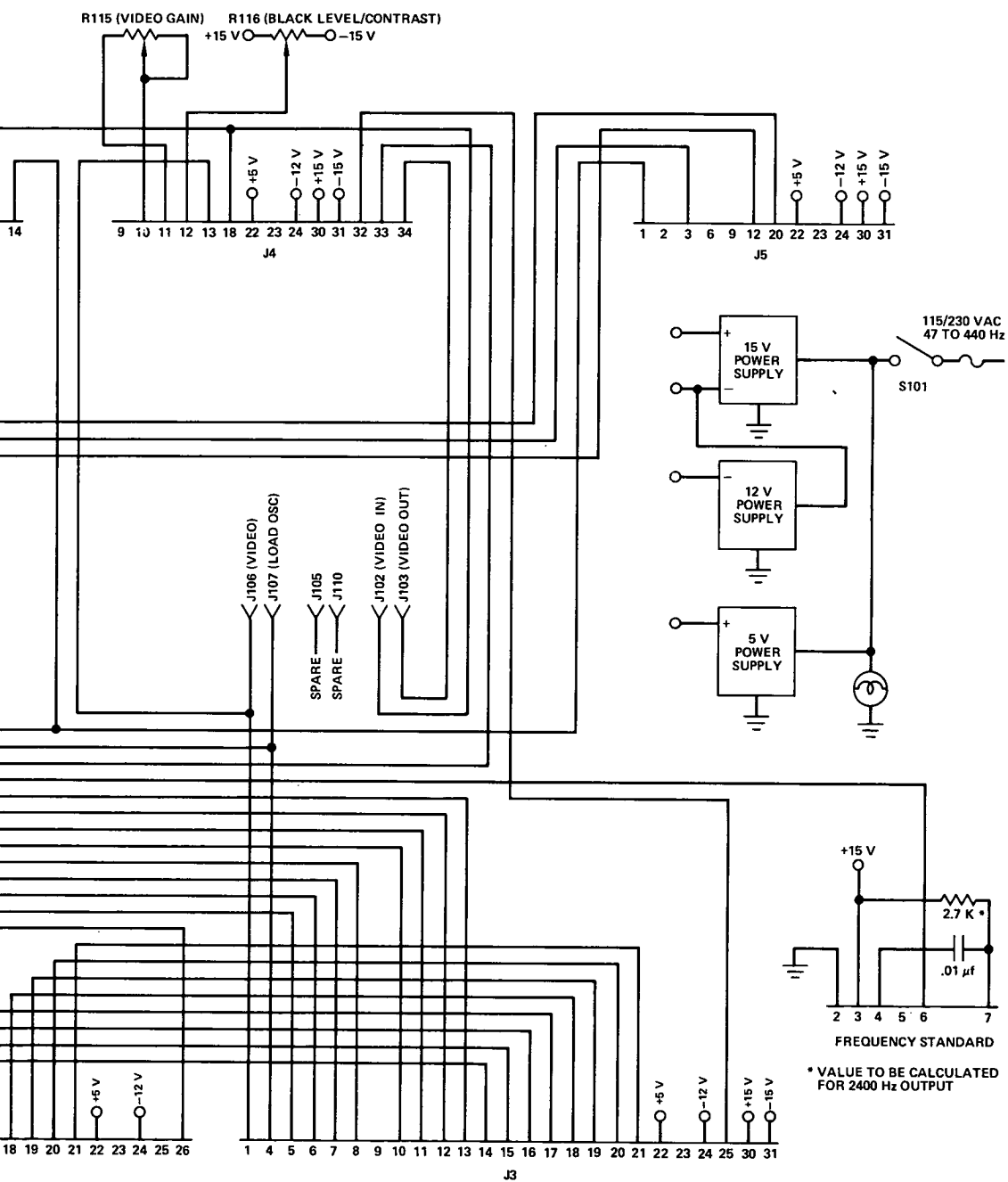


Figure 36. Chassis and Front Panel Wiring Diagram

Card 1

Refer to figure 25.

Dump Clock Calibration

1. Turn power switch to OFF.
2. Connect the Digital Frequency meter to pin 17 of Card 1.
3. Remove IC, U15.
4. Set pin 2 of U15 at +5 V.
5. Set the LINE RATE switch to 96.
6. Turn power switch to ON.
7. Adjust R18 until 1650 ± 10 Hz is read on the Digital Frequency meter.
8. Set LINE RATE switch to 120.
9. Adjust R16 until 2060 ± 10 Hz is read on the Digital Frequency meter.
10. Set LINE RATE switch to 240.
11. Adjust R14 until 4110 ± 10 Hz is read on the Digital Frequency meter.
12. Turn power switch to OFF.
13. Reinstall U15 after removing power from pin 2 of U15.

Load Start Calibration

1. Turn power switch to OFF.
2. Remove Card 6.
3. Connect oscilloscope to pin 3 of U1.
4. Connect oscillator to pin 1, Card 1.
5. Set oscillator to approximately 1 Hz.
6. Adjust gain of oscillator from zero until the output of U1 can be seen on the oscilloscope.
7. Set NORMAL/LIN COR switch to LIN COR.
8. Turn power switch to ON.
9. Replace R32 with a resistor that will adjust the pulse width of U1 to 29.6 m/s.
10. Turn power switch to OFF.
11. Replace Card 6.

Card 2

No calibration is required for Card 2.

Card 3

Refer to figure 19.

1. Turn power switch to OFF.
2. Remove Cards 1 and 4.
3. Connect d.c. voltage source, variable from -10 to +10 volts, to pin 1 of Card 3.
4. Connect the d.c. digital voltmeter to the output of the variable ± 10 volt power supply.
5. Connect pulse generator to pin 4 of Card 3.
6. Set the pulse rep rate at approximately 3000 Hz.
7. Set the pulse width of the pulse generator at approximately 10 μ s.
8. Connect the oscilloscope to pin 57 of U1.
9. Turn power switch to ON.
10. Adjust voltage on pin 4 of Card 3 to -10 volts.
11. Adjust R6 until a state change is observed on pin 57 of U1 monitored by the oscilloscope, only as the voltage crosses zero volts ± 5 mV, as the voltage is increased from -10 through zero volts. After crossing zero volts, a state change should be observed every 19.57 mV.
12. Set the voltage at pin 4 of U1 to 11 volts.
13. Adjust R2 until a state change is observed at pin 57 of U1 monitored on the oscilloscope, only as the voltage crosses 10 volts ± 5 mV, when the voltage is decreased from 11 volts through 10 volts. After crossing 10 volts, a state change should be observed for every decrease of 19.57 mV at pin 4 of U1.
14. There is an interplay between R2 and R6; therefore, steps 10, 11, 12, and 13 will have to be repeated until all interplay is removed.
15. Turn power switch to OFF.
16. Replace Cards 1 and 4.

Card 4

Refer to figure 18.

1. Turn power switch to OFF.
2. Connect special designed AM Modulator to pin 18 of Card 4.
3. Determine the maximum peak-to-peak signal level expected at pin 18 of Card 1 and adjust the output of the AM modulator to that value with approximately 100 percent modulation.
4. Set one oscillator at 2.4 kHz and the other at 100 Hz.
5. Connect oscilloscope to pin 10 of U2B.
6. Turn power switch to ON.
7. Adjust R5 so that the requirement specified in the Detailed Circuit Description section of Card 4 is met.
8. Turn power switch to OFF.
9. Connect oscilloscope to pin 12 of U3A.
10. Turn power switch to ON.
11. Adjust R1 such that the peak-to-peak voltage at pin 12 of U3A is 10 volts.
12. Turn power switch to OFF.
13. Apply 10 volts to pin 32 of Card 1.
14. Connect the oscilloscope to pin 12 of U4B.
15. Turn power switch to ON.
16. Adjust R24 so that the peak-to-peak voltage of pin 12 of U4B is 10 volts.
17. Adjust R39 to output a voltage representing white on the display monitor.
18. Turn power switch to OFF.

Card 5

Refer to figure 13.

1. Turn power switch to OFF.
2. Remove Card 1.
3. Connect the pulse generator to pin 3 of Card 5.
4. Set the pulse generator to a 1 Hz rep rate and the pulse width to 10 μ s.
5. Turn power switch to ON.
6. Adjust R4 such that the output of U1A, pin 12, meets the requirement as specified in the Detailed Circuit Description section of Card 5.

7. Also, adjust R13 to meet the specified requirements.
8. Turn power switch to OFF.
9. Remove U2 from Card 5.
10. From an external power supply, apply 10.3 volts d.c. \pm 5 mV to the junction of R24, R26, R28, and R30.
11. Turn power switch to ON.
12. Adjust R54 so that the output of U4B, pin 10, is -10.3 volts \pm 5 mV.
13. Turn power switch to OFF.
14. Replace Card 1.
15. Remove Card 6.
16. Connect the pulse generator at pin 1 of Card 1 and set the pulse generator rep rate at 1 Hz and the pulse width at 10 μ s.
17. Connect pin 3 of Card 1 to the external sync input on the oscilloscope.
18. Connect the output of U4A to one input of the dual-trace oscilloscope and the output of U5, pin 15, to the other input.
19. Turn power switch to ON.
20. Adjust R35 of Card 5 so that the reset pulse of Card 1 is coincident with the return of the output of U4A, pin 12, to 10.3 volts.
21. Turn power switch to OFF.
22. Replace Card 6.

Card 6

Refer to figure 7.

1. Connect the oscilloscope to LOAD OSC front panel output jack.
2. Connect data signal to the front panel VIDEO input jack at the level used to calibrate Card 1.
3. Turn power switch to ON.
4. Set the front panel IR/VIS switch to IR.
5. Adjust R33 until load pulses are seen on the oscilloscope.
6. Set the Front Panel IR/VIS switch to VIS.

7. Adjust R35 until load pulses are seen on the oscilloscope.
8. Repeat steps 4, 5, 6, and 7 until the load pulses are seen on both IR and VIS with no further adjustment of R33.

Goddard Space Flight Center
National Aeronautics and Space Administration
Greenbelt, Maryland April 1975

REFERENCES

1. Charles H. Vermillion, Weather Satellite Picture Receiving Stations—Inexpensive Construction of Automatic Picture Transmission Ground Equipment, NASA SP-5080, 1969.

APPENDIX A

DERIVATION OF THE PANORAMIC DISTORTION COMPENSATION FUNCTION

The geometric distortion caused by sensor scan and earth curvature can be removed from the scan normal to the orbit track by any of several operations performed at the ground station or in the spacecraft and with the data in either analog or digital form. The methods for geometric correction to compensate for earth curvature are pixel* stretching, linear interpolation, and extra element insertion; all three methods use a "piece-wise" expansion scheme. A detailed explanation of these methods may be found in "The Final Report, Low Cost VHRR/AVHRR Ground Station Study Program," April 10, 1974. The geometric correction technique used in this scan converter and discussed in the following paragraphs will be a form of the pixel stretching method.

Figure A-1 illustrates the geometry of the spacecraft and earth and shows how the panoramic distortion of each scan of the radiometer is generated. It is obvious by inspection that as θ changes at a constant rate, $ds/d\theta$ increases from some finite number to infinity at the earth's edge. Pixel stretching in this system is accomplished by generating a frequency and time function where frequency is proportional to $ds/d\theta$ and time is proportional to θ . Implementing this technique is relatively simple and does not have the inherent distortion found in the element insertion and linear interpolation methods. In this method each pulse period represents the same length of earth surface and is limited only by the resolution of the spacecraft scanner (pixel size) and bandwidth of the telemetry.

Generating the function $ds/d\theta$,

$$\begin{aligned}\psi &= 90^\circ - \theta + \phi, \\ \phi &= \psi + \theta - 90^\circ, \\ X &= R \cos \phi,\end{aligned}$$

and

$$\begin{aligned}\cos \phi &= \cos (\psi + \theta - 90^\circ) = \sin (\psi + \theta) \\ &= \sin \psi \cos \theta + \cos \psi \sin \theta.\end{aligned}\tag{1}$$

Using the Law of Sines,

$$\begin{aligned}\frac{\sin \theta}{R} &= \frac{\sin \psi}{A + R}, \\ \sin \psi &= \frac{A + R}{R} \sin \theta,\end{aligned}\tag{2}$$

*Picture element.

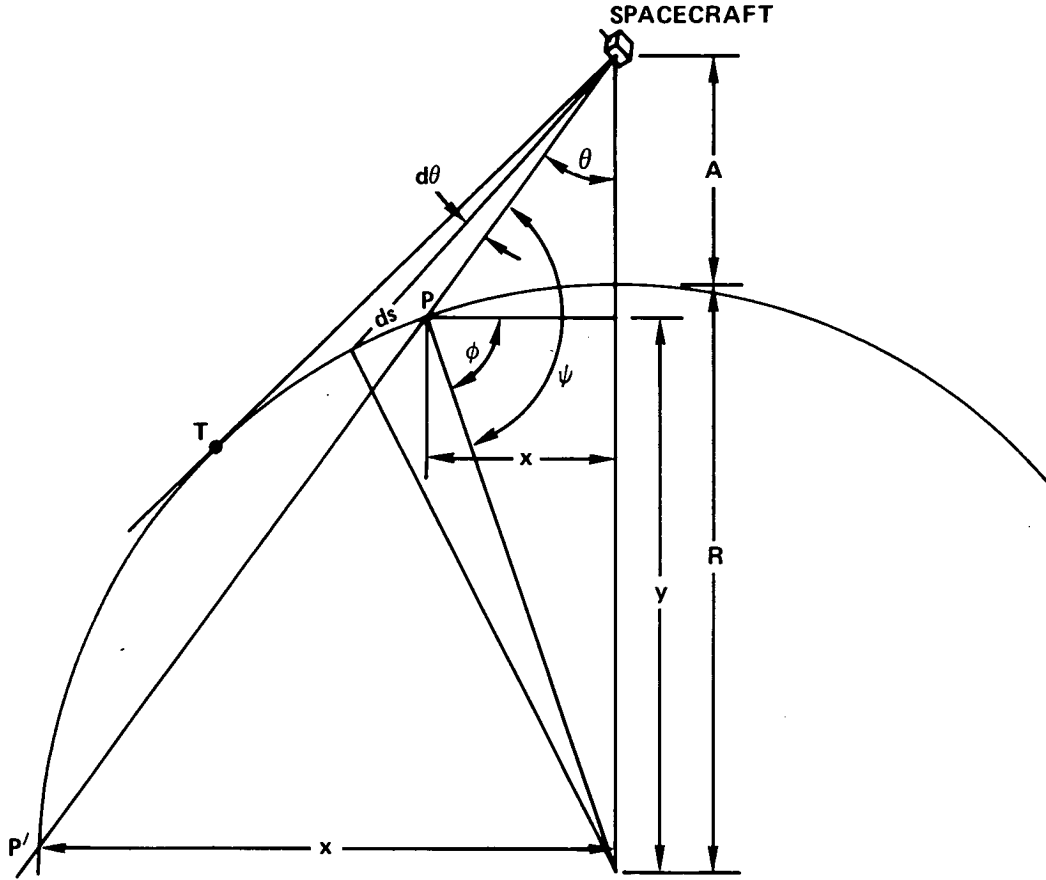


Figure A-1. Spacecraft and Earth Geometry

$$\sin^2 \psi = \frac{(A + R)^2}{R^2} \sin^2 \theta, \quad (3)$$

and

$$\cos^2 \psi = 1 - \sin^2 \psi. \quad (4)$$

Substituting equation 3 into equation 4 yields

$$\begin{aligned} \cos^2 \psi &= 1 - \frac{(A + R)^2}{R^2} \sin^2 \theta \\ &= \frac{R^2 - (A + R)^2 \sin^2 \theta}{R^2} \end{aligned}$$

and

$$\cos \psi = \pm \frac{1}{R} [R^2 - (A + R)^2 \sin^2 \theta]^{1/2}. \quad (5)$$

By inspection of figure A-1 it is seen that

$$X = R \cos \phi. \quad (6)$$

Substituting equation 1 into equation 6,

$$X = R[\sin \psi \cos \theta + \cos \psi \sin \theta]. \quad (7)$$

By substituting equation 2 and 5 into equation 7, equation 7 reduces to

$$X = (A + R) \sin \theta \cos \theta \pm [R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}} \sin \theta,$$

which further reduces to

$$X = \frac{1}{2} (A + R) \sin 2\theta \pm [R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}} \sin \theta. \quad (8)$$

For any given angle θ , X will take on two values, one at P and the other P' except at the tangent point (T) (figure A-1). Because only the $ds/d\theta$ of the earth surface facing the spacecraft is pertinent to this problem, and, as Figure A-1 shows, this is the smaller value of X , the positive sign will be dropped. Therefore,

$$X = \frac{1}{2} (A + R) \sin 2\theta - [R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}} \sin \theta \quad (9)$$

$$\frac{dx}{d\theta} = (A + R) \cos 2\theta - \cos \theta [R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}}$$

$$- \frac{\frac{1}{2} [-2 (A + R)^2 \sin \theta \cos \theta] \sin \theta}{[R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}}}$$

$$= (A + R) \cos 2\theta - \frac{[R^2 - (A + R)^2 \sin^2 \theta - (A + R)^2 \sin^2 \theta] \cos \theta}{[R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}}}$$

and

$$\frac{dx}{d\theta} = (A + R) \cos 2\theta - \frac{[R^2 - 2(A + R)^2 \sin^2 \theta] \cos \theta}{[R^2 - (A + R)^2 \sin^2 \theta]^{\frac{1}{2}}} \quad (10)$$

By inspection of figure A-1, it can be seen that

$$(ds)^2 = (dx)^2 + (dy)^2,$$

$$\left(\frac{ds}{dx}\right)^2 = 1 + \left(\frac{dy}{dx}\right)^2,$$

$$\frac{ds}{dx} = \sqrt{1 + \left(\frac{dy}{dx}\right)^2},$$

and

$$x^2 + y^2 = R^2. \quad (11)$$

Differentiating equation 11 and solving for dy/dx ,

$$2xdx + 2ydy = 0,$$

$$\frac{dy}{dx} = -\frac{x}{y},$$

$$\left(\frac{dy}{dx}\right)^2 = \left(\frac{x}{y}\right)^2 = \frac{x^2}{R^2 - x^2},$$

and

$$\begin{aligned}\frac{ds}{dx} &= \sqrt{1 + \frac{x^2}{R^2 - x^2}}, \\ &= \sqrt{\frac{R^2}{R^2 - x^2}}.\end{aligned}\quad (12)$$

Substituting equation 9 into equation 12,

$$\frac{ds}{dx} = \left[\frac{R^2}{R^2 - \left[\frac{1}{2} (A + R) \sin 2\theta - [R^2 - (A + R)^2 \sin^2 \theta]^{1/2} \sin \theta \right]^2} \right]^{1/2} \quad (13)$$

and

$$\frac{ds}{d\theta} = \frac{ds}{dx} \cdot \frac{dx}{d\theta}. \quad (14)$$

Substituting equations 10 and 13 into equation 14,

$$\begin{aligned}\frac{ds}{d\theta} &= \left[\frac{R^2}{R^2 - \left[\frac{1}{2} (A + R) \sin 2\theta - [R^2 - (A + R)^2 \sin^2 \theta]^{1/2} \sin \theta \right]^2} \right] \times \\ &\quad \left[(A + R) \cos 2\theta - \frac{R^2 - 2(A + R)^2 \sin^2 \theta \cos \theta}{[R^2 - (A + R)^2 \sin^2 \theta]^{1/2}} \right].\end{aligned}\quad (15)$$

The application of $ds/d\theta$ in this system is one of scaling the pixel at any angle θ to the pixel at nadir. Therefore, it is obvious that $ds/d\theta$ is normalized by determining $ds/d\theta$ at $\theta = 0^\circ$ and dividing equation 10 by that value.

By inserting 0 for θ into equation 15,

$$\frac{ds}{d\theta}_{\text{nadir}} = \left[\frac{R^2}{R^2} \right] \left[(A + R) - \frac{R^2}{[R^2]^{1/2}} \right] = A,$$

$$\frac{ds}{d\theta_{\text{nadir}}} = A,$$

and

$$\frac{ds}{d\theta_{\text{norm}}} = \frac{\frac{ds}{d\theta}}{A}.$$

The correction curve $ds/d\theta_{\text{norm}}$ is dependent on the altitude of the orbiting spacecraft. It is necessary, therefore, to determine a correction curve representative of each spacecraft monitored. The solution of equation 15 is a rigorous task if done by hand. Therefore, the following simple program which solves equation 15 has been included.

```

CONTROL T
MAINPROGRAM FORT
WRITE (6,70)
70 FORMAT (1H1//5X,$SCAN HALF ANGLES 5X $CORRECTIONS,5X,$EARTH NORMAL
*$,5X,$EARTH NORMAL ANGLE CHANGES,5X,$EARTH SURFACE ANGLE CHANGES/)
A= 780.
R= 3437.5
AINC = 0.0
TMIN = 0.0
TMAX = ASIN(R/(A+R))
DELT = (TMAX)/100.
99 B= SQRT (R*R-(A+R)**2*SIN(AINC)*SIN(AINC))
C= R*R -2.*(A+R)**2*SIN(AINC)*SIN(AINC)
Y= 0.5*(A+R)*SIN(2.*AINC)-B*SIN(AINC)
YP=(A+R)*COS(2.*AINC)-C*COS(AINC)/B
SP=YP*SQRT(R*R/(R*R-Y*Y))
SPNORM = SP/A
WRITE (6,20) AINC,SPNORM,Y,YP,SP
20 FORMAT (E19.6,E16.6,E17.6,E27.6,E31.6)
AINC=AINC+DELT
IF(AINC.GT.TMAX) GO TO 100
GO TO 99
100 WRITE (6,30) TMAX
30 FORMAT (///10X,$THE MAXIMUM SCAN HALF ANGLE !S$,E14.6)
STOP
END
SPECIAL ALLOC.
SUBROUTINES
        ASIN
        SQRT
        SIN
        COS
CONSTANTS
CMN BLK NAMES
EQUV. ALLOC.
SCALAR ALLOC
        FORT
        A
        R
        AINC
        TMIN
        TMAX
        DELT
        B
        C
        Y
        YP
        SP
        SPNORM
ARRAY ALLOC
TEMP

```

SCAN HALF ANGLE	CORRECTION	EARTH NORMAL	EARTH NORMAL ANGLE CHANGE	EARTH SURFACE ANGLE CHANGE
0.952816E-02	0.100000E01	0.700000E03	0.700000E03	0.700000E03
0.100563E-01	0.100012E01	0.700095E03	0.700095E03	0.700097E03
0.265045E-01	0.100050E01	0.700380E03	0.700380E03	0.700307E03
0.381120E-01	0.100112E01	0.700655E03	0.700655E03	0.700671E03
0.476008E-01	0.100199E01	0.701521E03	0.701521E03	0.701550E03
0.571690E-01	0.100311E01	0.702378E03	0.702378E03	0.702424E03
0.666971E-01	0.100448E01	0.703426E03	0.703426E03	0.703495E03
0.762253E-01	0.100601E01	0.704672E03	0.704672E03	0.704762E03
0.857535E-01	0.100799E01	0.706106E03	0.706106E03	0.706229E03
0.952816E-01	0.101012E01	0.707746E03	0.707746E03	0.707896E03
0.104881E00	0.101242E01	0.709590E03	0.709590E03	0.709706E03
0.114330E00	0.101491E01	0.711615E03	0.711615E03	0.711641E03
0.123800E00	0.101751E01	0.713835E03	0.713835E03	0.714123E03
0.133394E00	0.102024E01	0.716290E03	0.716290E03	0.716615E03
0.142922E00	0.102311E01	0.718944E03	0.718944E03	0.719328E03
0.152451E00	0.102612E01	0.721808E03	0.721808E03	0.722241E03
0.161974E00	0.102928E01	0.724892E03	0.724892E03	0.725361E03
0.171501E00	0.103259E01	0.728205E03	0.728205E03	0.728531E03
0.181030E00	0.103606E01	0.731747E03	0.731747E03	0.732066E03
0.190560E00	0.103969E01	0.735527E03	0.735527E03	0.735797E03
0.200091E00	0.104349E01	0.739548E03	0.739548E03	0.739924E03
0.209624E00	0.104746E01	0.743811E03	0.743811E03	0.744349E03
0.219144E00	0.105160E01	0.748317E03	0.748317E03	0.748906E03
0.228670E00	0.105591E01	0.753067E03	0.753067E03	0.753644E03
0.238204E00	0.106039E01	0.758063E03	0.758063E03	0.758664E03
0.247734E00	0.106504E01	0.763307E03	0.763307E03	0.764005E03
0.257264E00	0.106986E01	0.768800E03	0.768800E03	0.769655E03
0.266794E00	0.107486E01	0.774543E03	0.774543E03	0.775516E03
0.276324E00	0.108004E01	0.780546E03	0.780546E03	0.781696E03
0.285854E00	0.108539E01	0.786810E03	0.786810E03	0.788097E03
0.295384E00	0.109091E01	0.793345E03	0.793345E03	0.794719E03
0.304914E00	0.109661E01	0.800151E03	0.800151E03	0.801570E03
0.314444E00	0.110249E01	0.807230E03	0.807230E03	0.808655E03
0.323974E00	0.110855E01	0.814583E03	0.814583E03	0.815976E03
0.333504E00	0.111479E01	0.822218E03	0.822218E03	0.823536E03
0.343034E00	0.112120E01	0.830139E03	0.830139E03	0.831346E03
0.352564E00	0.112779E01	0.838356E03	0.838356E03	0.839406E03
0.362094E00	0.113456E01	0.846879E03	0.846879E03	0.847716E03
0.371624E00	0.114151E01	0.855708E03	0.855708E03	0.856276E03
0.381154E00	0.114864E01	0.864853E03	0.864853E03	0.865086E03
0.390684E00	0.115595E01	0.874314E03	0.874314E03	0.874146E03
0.400214E00	0.116344E01	0.884093E03	0.884093E03	0.883456E03
0.409744E00	0.117111E01	0.894192E03	0.894192E03	0.892916E03
0.419274E00	0.117896E01	0.904613E03	0.904613E03	0.893526E03
0.428804E00	0.118700E01	0.915356E03	0.915356E03	0.894286E03
0.438334E00	0.119523E01	0.926421E03	0.926421E03	0.895196E03
0.447864E00	0.120365E01	0.937816E03	0.937816E03	0.896256E03
0.457394E00	0.121226E01	0.949541E03	0.949541E03	0.897466E03
0.466924E00	0.122106E01	0.961596E03	0.961596E03	0.898826E03
0.476454E00	0.123004E01	0.973981E03	0.973981E03	0.899336E03
0.485984E00	0.123920E01	0.986696E03	0.986696E03	0.900006E03
0.495514E00	0.124854E01	0.999741E03	0.999741E03	0.900836E03
0.505044E00	0.125806E01	0.101100E04	0.101100E04	0.901826E03
0.514574E00	0.126776E01	0.102483E04	0.102483E04	0.902976E03
0.524104E00	0.127764E01	0.103890E04	0.103890E04	0.904296E03
0.533634E00	0.128770E01	0.105321E04	0.105321E04	0.905786E03
0.543164E00	0.129794E01	0.106776E04	0.106776E04	0.907446E03
0.552694E00	0.130836E01	0.108256E04	0.108256E04	0.909276E03
0.562224E00	0.131896E01	0.109761E04	0.109761E04	0.911276E03
0.571754E00	0.132974E01	0.111291E04	0.111291E04	0.913446E03
0.581284E00	0.134069E01	0.112816E04	0.112816E04	0.915786E03
0.590814E00	0.135181E01	0.114361E04	0.114361E04	0.918296E03
0.600344E00	0.136311E01	0.115926E04	0.115926E04	0.920976E03
0.609874E00	0.137459E01	0.117511E04	0.117511E04	0.923826E03
0.619404E00	0.138624E01	0.119116E04	0.119116E04	0.926846E03
0.628934E00	0.139806E01	0.120741E04	0.120741E04	0.929936E03
0.638464E00	0.141006E01	0.122386E04	0.122386E04	0.933106E03
0.647994E00	0.142224E01	0.124051E04	0.124051E04	0.936446E03
0.657524E00	0.143459E01	0.125746E04	0.125746E04	0.939956E03
0.667054E00	0.144711E01	0.127471E04	0.127471E04	0.943636E03
0.676584E00	0.145979E01	0.129226E04	0.129226E04	0.947486E03
0.686114E00	0.147264E01	0.131011E04	0.131011E04	0.951506E03
0.695644E00	0.148566E01	0.132816E04	0.132816E04	0.955696E03
0.705174E00	0.149884E01	0.134641E04	0.134641E04	0.960056E03
0.714704E00	0.151219E01	0.136486E04	0.136486E04	0.964586E03
0.724234E00	0.152571E01	0.138351E04	0.138351E04	0.969286E03
0.733764E00	0.153939E01	0.140236E04	0.140236E04	0.974146E03
0.743294E00	0.155324E01	0.142141E04	0.142141E04	0.979166E03
0.752824E00	0.156726E01	0.144066E04	0.144066E04	0.984346E03
0.762354E00	0.158144E01	0.146011E04	0.146011E04	0.989686E03
0.771884E00	0.159579E01	0.147976E04	0.147976E04	0.995186E03
0.781414E00	0.161030E01	0.149961E04	0.149961E04	0.100746E04
0.790944E00	0.162497E01	0.151966E04	0.151966E04	0.101366E04
0.800474E00	0.163979E01	0.153991E04	0.153991E04	0.102046E04
0.810004E00	0.165477E01	0.156036E04	0.156036E04	0.102786E04
0.819534E00	0.166991E01	0.158101E04	0.158101E04	0.103586E04
0.829064E00	0.168521E01	0.160186E04	0.160186E04	0.104446E04
0.838594E00	0.170066E01	0.162291E04	0.162291E04	0.105366E04
0.848124E00	0.171626E01	0.164416E04	0.164416E04	0.106346E04
0.857654E00	0.173201E01	0.166561E04	0.166561E04	0.107386E04
0.867184E00	0.174791E01	0.168726E04	0.168726E04	0.108486E04
0.876714E00	0.176396E01	0.170911E04	0.170911E04	0.109646E04
0.886244E00	0.178016E01	0.173116E04	0.173116E04	0.110866E04
0.895774E00	0.179651E01	0.175341E04	0.175341E04	0.112146E04
0.905304E00	0.181301E01	0.177586E04	0.177586E04	0.113486E04
0.914834E00	0.182966E01	0.179851E04	0.179851E04	0.114886E04
0.924364E00	0.184646E01	0.182136E04	0.182136E04	0.116346E04
0.933894E00	0.186341E01	0.184441E04	0.184441E04	0.117866E04
0.943424E00	0.188051E01	0.186766E04	0.186766E04	0.119446E04
0.952954E00	0.189776E01	0.189111E04	0.189111E04	0.121086E04
0.962484E00	0.191516E01	0.191476E04	0.191476E04	0.122786E04
0.972014E00	0.193271E01	0.193851E04	0.193851E04	0.124546E04
0.981544E00	0.195041E01	0.196246E04	0.196246E04	0.126366E04
0.991074E00	0.196826E01	0.198661E04	0.198661E04	0.128246E04
1.000604E00	0.198626E01	0.201096E04	0.201096E04	0.130186E04
1.010134E00	0.200441E01	0.203551E04	0.203551E04	0.132186E04
1.019664E00	0.202271E01	0.206026E04	0.206026E04	0.134246E04
1.029194E00	0.204116E01	0.208521E04	0.208521E04	0.136366E04
1.038724E00	0.205976E01	0.211036E04	0.211036E04	0.138546E04
1.048254E00	0.207851E01	0.213581E04	0.213581E04	0.140786E04
1.057784E00	0.209741E01	0.216151E04	0.216151E04	0.143086E04
1.067314E00	0.211646E01	0.218746E04	0.218746E04	0.145446E04
1.076844E00	0.213556E01	0.221366E04	0.221366E04	0.147866E04
1.086374E00	0.215481E01	0.224011E04	0.224011E04	0.150346E04
1.095904E00	0.217421E01	0.226681E04	0.226681E04	0.152886E04
1.105434E00	0.219376E01	0.229376E04	0.229376E04	0.155486E04
1.114964E00	0.221346E01	0.232096E04	0.232096E04	0.158146E04
1.124494E00	0.223331E01	0.234841E04	0.234841E04	0.160866E04
1.134024E00	0.225331E01	0.237611E04	0.237611E04	0.163646E04
1.143554E00	0.227346E01	0.240406E04	0.240406E04	0.166486E04
1.153084E00	0.229376E01	0.243226E04	0.243226E04	0.169386E04
1.162614E00	0.231421E01	0.246071E04	0.246071E04	0.172346E04
1.172144E00	0.233481E01	0.248941E04	0.248941E04	0.175366E04
1.181674E00	0.235556E01	0.251836E04	0.251836E04	0.178446E04
1.191204E00	0.237646E01	0.254756E04	0.254756E04	0.181586E04
1.200734E00	0.239751E01	0.257691E04	0.257691E04	0.184786E04
1.210264E00	0.241871E01	0.260641E04	0.260641E04	0.188046E04
1.219794E00	0.243996E01	0.263606E04	0.263606E04	0.191366E04
1.229324E00	0.246136E01	0.266586E04	0.266586E04	0.194746E04
1.238854E00	0.248291E01	0.269591E04	0.269591E04	0.198186E04
1.248384E00	0.250461E01	0.272611E04	0.272611E04	0.201686E04
1.257914E00	0.252646E01	0.275646E04	0.275646E04	0.205246E04
1.267444E00	0.254846E01	0.278696E04	0.278696E04	0.208866E04
1.276974E00	0.257061E01	0.281761E04	0.281761E04	0.212546E04
1.286504E00	0.259291E01	0.284841E04	0.284841E04	0.216286E04
1.296034E00	0.261536E01	0.287936E04	0.287936E04	0.220086E04
1.305564E00	0.263796E01	0.291046E04	0.291046E04	0.223946E04
1.315094E00	0.266071E01	0.294171E04	0.294171E04	0.227866E04
1.324624E00	0.268361E01	0.297311E04	0.297311E04	0.231846E04
1.334154E00	0.270666E01	0.300466E04	0.300466E04	0.235886E04
1.343684E00	0.272986E01	0.303636E04	0.303636E04	0.239986E04
1.353214E00	0.275321E01	0.306821E04	0.306821E04	0.244146E04
1.362744E00	0.277671E01	0.310021E04	0.310021E04	0.248366E04
1.372274E00	0.280036E01	0.313236E04	0.313236E04	0.252646E04
1.381804E00	0.282416E01	0.316466E04	0.	

APPENDIX B

WAVE SHAPING NETWORK CALCULATIONS

INTRODUCTION

To correct for geographic panoramic distortion, the wave shaping network of the panoramic distortion correction card (card 5) of the scan converter must be tailored to the orbit of the spacecraft being monitored. Appendix A illustrates how to generate the correction function $ds/d\theta$ and this appendix will show how to implement it. The following is a design procedure which could be followed to design a network which will generate the desired correction curve. This example uses an orbit of 1443 km (780 nmi) above the earth's surface and an earth radius of 6359.4 km (3437.5 nmi).

PROCEDURE

An accurate curve must be plotted from the computer printout data in Appendix A as shown in figure B-1, and then the portion of the earth's surface to be analyzed must be determined. (In this example, 90 percent of the surface was chosen.) Five line segments fitted for minimum error must be laid out, and the points of intersection of the line segments found (see figure B-1). For this example, these points are as shown in Table B-1.

Table B-1
Angular Displacement vs. Rate Change of Earth's Surface, Absolute Values

θ	ds/dt norm
0.0	1.01
0.2	1.01
0.43	1.28
0.615	1.82
0.77	2.96
0.855	4.74

Because θ changes at a constant rate, it is proportioned to time. In an analog system, if an operation is to be performed on a function, the function should be represented by a voltage, and θ is no exception to this rule. A ramp generator is used to accomplish this function. Because $ds/d\theta$ is the same for either plus or minus values of θ , the ramp generator is designed to be symmetrical about the nadir point. Figure B-2 depicts this, showing the desired voltage versus θ values representing the breakpoints of the approximate correction curve of figure B-1. The maximum angle of 0.855 rad will be represented by 10.3 V because this is the maximum output of amplifier U1B of the panoramic distortion correction card (card 5). The angular displacement θ represented as a voltage vs. the rate change of the earth's surface represented as a current is shown in Table B-2.

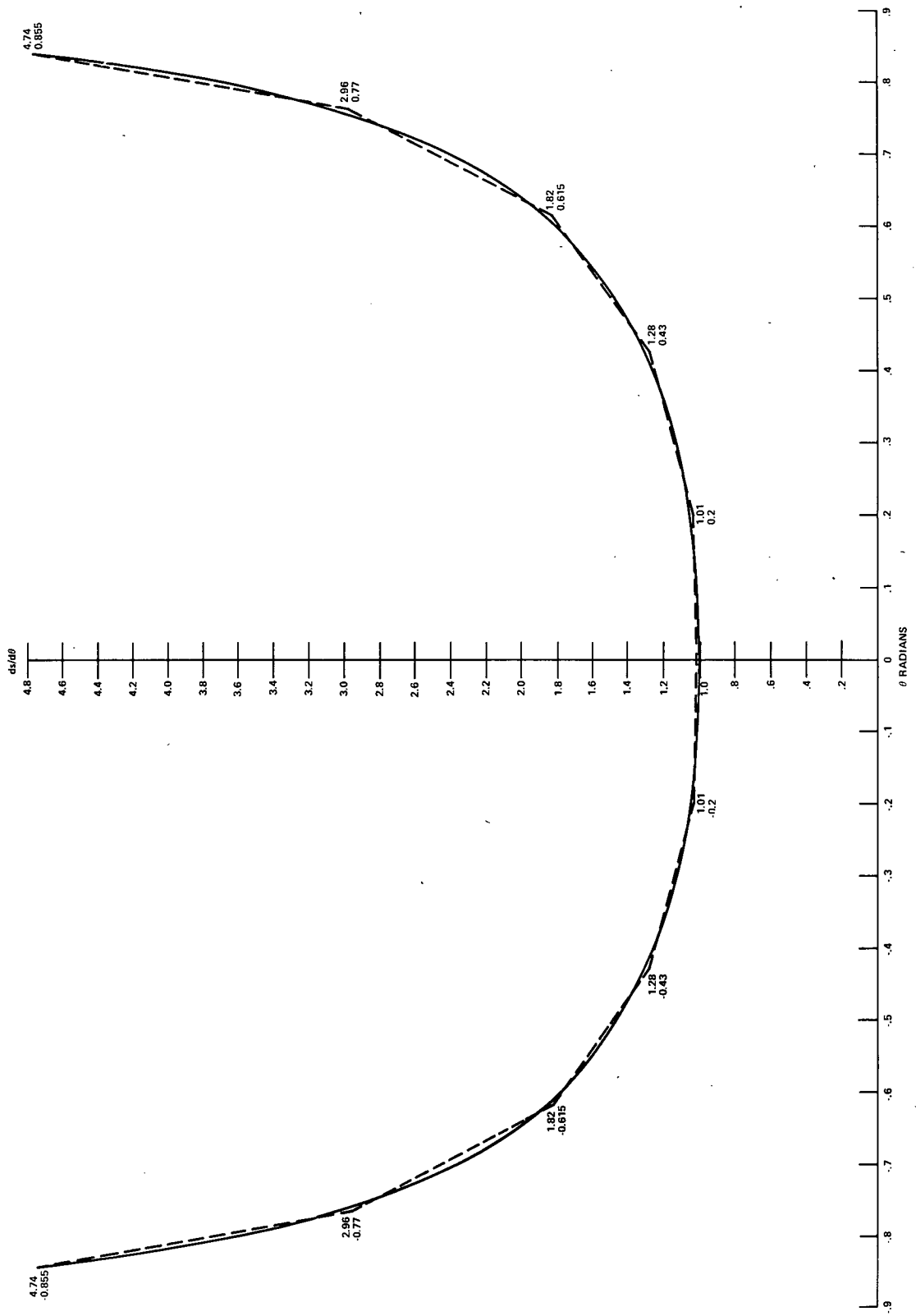


Figure B-1. Curve from Computer Printout Data

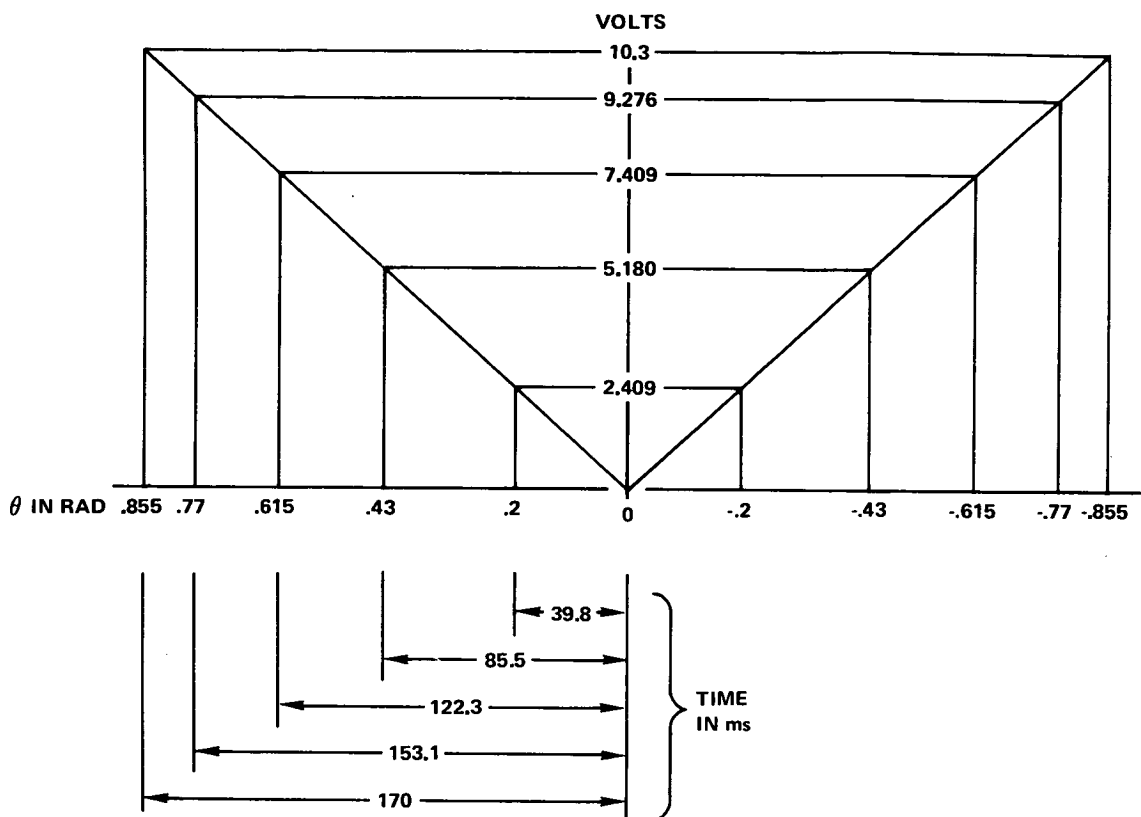


Figure B-2. Correction Curve Breakpoints

The intermediate values of θ were calculated by the following equation:

$$\frac{V_{in.}}{10.3} = \frac{\theta}{8.55} \quad (1)$$

$$V_{in} = \frac{10.3}{8.55} \theta$$

After generating a voltage function representing θ , it will be necessary to generate a function representing the correction curve itself. This is accomplished by diodes which switch in resistor networks, changing the rate of current into the summing operational amplifier U3A (see figure B-3).

The current out of the first network is arbitrary and was selected to be $100 \mu\text{A}$ when the voltage across the resistor network is 5.180 V. The other values were calculated using equation 9.

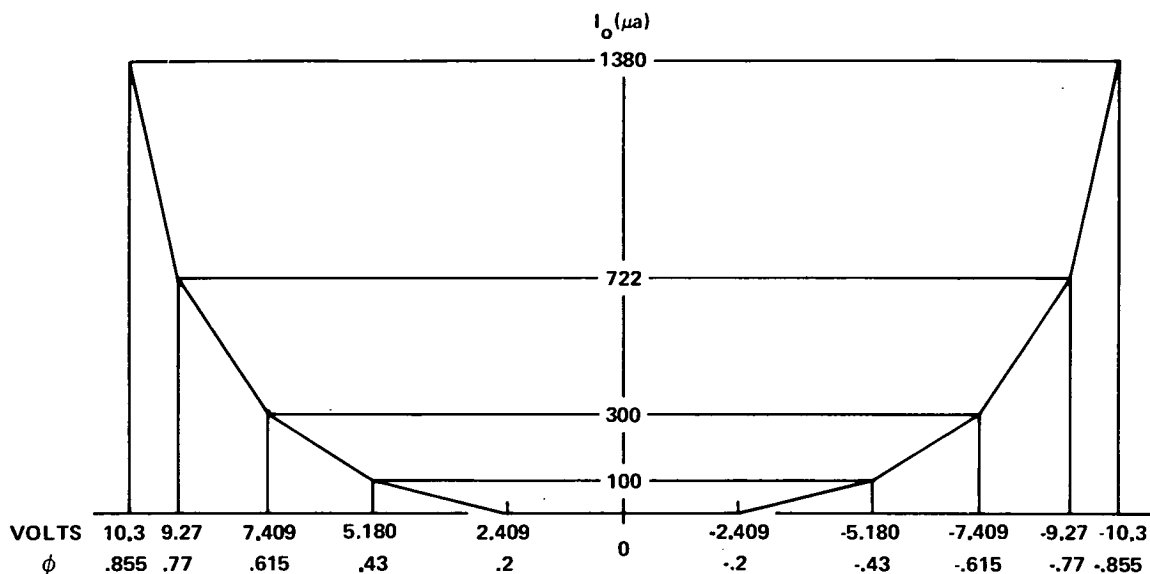


Figure B-3. V_{in} versus I_o Out of the Diode Network

Table B-2

Angular Displacement θ vs. Rate Change of Earth's Surface, Representative Values

θ	V_{in}	I_o
0	0	0
0.2	2.409	0
0.43	5.180	100
0.615	7.409	300
0.77	9.27	722
0.855	10.3	1380

RESISTOR NETWORK CALCULATIONS

Table B-3 shows the portion of the total current that each resistor network of the diode shaper supplies to the input of the summing operational amplifier at the specified breakpoint. (The values were carried out to four places to avoid accumulation of errors in calculations.) Figure B-4 shows the basic resistor network.

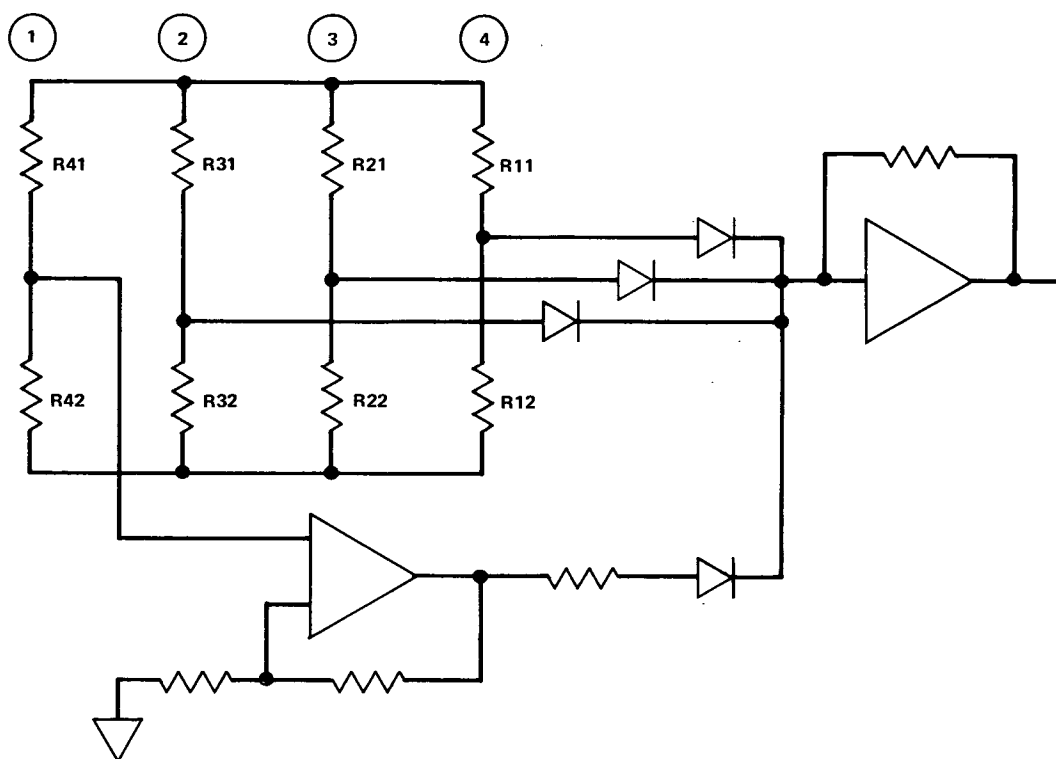


Figure B-4. Basic Resistor Network

Table B-3
Breakpoints of Resistor Network

Stage	Voltage Breakpoints				
	2.409	5.18	7.409	9.276	10.3
*	0	100	299.8	721.85	1380.7
I	0	100	200.22	284.67	331.07
II	0	0	99.68	217.86	283.34
III	0	0	0	219.32	421.23
IV	0	0	0	0	345.06

*Total current out of the diode shaping network.

The diodes selected were of the IN4446 type and have the following voltage current characteristics:

$$e_D = \frac{\ln(I_D \times 10^9)}{10 \ln 10} \quad (2)$$

where e_D is the forward drop across the diode with I_D (the forward current) flowing through it. The current provided by each leg of the shaping network is shown in figure B-5.

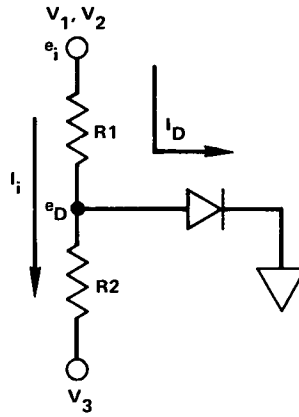


Figure B-5. Shaping Network Current

Because the current from each resistor network is fed into the input of a summing operational amplifier (figure B-4), and because the input to a summing operational amplifier may be taken to be ground potential, the cathodes of the diodes are considered to be at ground potential. V_1 represents the potential at e_L when e_D is at ground potential, and V_2 represents the potential at e_L when e_D is above ground potential. When e_D equals ground potential,

$$\frac{V_1}{R_1} = \frac{V_3}{R_2},$$

or

$$\frac{1}{R_2} = \frac{V_1}{V_3 R_1} \quad (3)$$

when $e_D > \text{ground potential}$.

$$V_2 = (I_1 + I_D) R_1 + e_D \quad (4)$$

and

$$I_1 R_2 = V_3 + e_D, \quad (5)$$

$$I_1 = \frac{V_3 + e_D}{R_2},$$

Substituting equation 5 into equation 4,

$$V_2 = R_1 \left[\frac{V_3 + e_D}{R_2} + I_D \right] + e_D, \quad (6)$$

and substituting equation 3 into equation 6,

$$\begin{aligned} V_2 &= R_1 \left[\frac{V_1}{V_3 R_1} (V_3 + e_D) + I_D \right] + e_D, \\ &= \frac{V_1}{V_3} (V_3 + e_D) + I_D R_1 + e_D, \end{aligned}$$

$$V_2 = V_1 + \frac{V_1 e_D}{V_3} + e_D + I_D R_1,$$

$$V_2 = V_1 + \left(\frac{V_1}{V_3} + 1 \right) e_D + I_D R_1,$$

solving for R_1

$$R_1 = \frac{V_2 - V_1 - \left(\frac{V_1}{V_3} + 1 \right) e_D}{I_D}. \quad (7)$$

solving for I_D

$$I_D = \frac{V_2 - V_1 - \left(\frac{V_1}{V_3} + 1 \right) e_D}{R_1} \quad (8)$$

Substituting equation 2 into equation 7,

$$R_1 = \frac{V_2 - V_1 - \left(\frac{V_1}{V_3} + 1 \right) \left[\frac{\ln(10^9 I_D)}{10 \ln 10} \right]}{I_D}.$$

Substituting equation 2 into equation 8

$$I_D = V_2 - V_1 - \left(\frac{V_1}{V_2} + 1 \right) \left[\frac{\ln(10^9 I_D)}{10 \ln 10} \right] \quad (9)$$

CALCULATING STAGE 1

$$V_1 = 2.409$$

$$V_2 = 5.18$$

$$V_3 = 15$$

$$I_D = 10^{-4}$$

$$R_1 = \frac{V_2 - V_1 - \left[\frac{V_1}{V_3} + 1 \right] \frac{\ln 10^{-4} \cdot 10^9}{10 \ln 10}}{10^{-4}}$$

$$= \frac{5.18 - 2.409 - \left[\frac{2.409}{15} + 1 \right] \frac{\ln 10^5}{10 \ln 10}}{10^{-4}} = 21907$$

$$R_1 \approx 21.9 \text{ k}\Omega$$

$$R_2 = \frac{V_3}{V_1} R_1 = \frac{15}{2.407}$$

$$R_2 \approx 136 \text{ k}\Omega$$

The current through resistor network No. 1 must now be calculated for the other break-point voltages of the other resistor networks. Because the current in resistor network No. 1 is not known for the other breakpoint voltages and as a direct solution for I_D in equation 7 is nearly impossible, the trial-and-error approach was used.

The steps in the trial-and-error method are as follows:

- (1) Let e_D equal 0.5 V.
- (2) Calculate I_D from equation 7.
- (3) With the resulting I_D of step 2, calculate I_D from equation 7.
- (4) Repeat steps 2 and 3 until the value of e_D and I_D satisfies both equations 2 and 7.

An inspection of equation 2 shows that the value of e_D is only slightly changed with a large change of current (I_D) in the region of $100 \mu\text{a}$. For this reason, the solution converges very rapidly and may be completed in as few as four iterations.

The calculations for I_D in stage 1 at the 7.409-V breakpoint are as follows:

First approximation is

$$I_D = \frac{V_2 - V_1 - \left[\frac{V_1}{V_3} + 1 \right] e_D}{R_1}$$

$$e_D = \frac{\ln \frac{I_D}{10^{-9}}}{\ln 10^{+0}}$$

$$I_D = \frac{7.409 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.5}{21.9 \times 10^3}$$

$$I_D = 2.01812 \times 10^{-4}$$

$$e_D = \frac{\ln \frac{2.01812 \times 10^{-4}}{10^{-9}}}{\ln 10^{10}}$$

$$e_D = 0.5305.$$

Second approximation is

$$I_D = \frac{7.409 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.5305}{21.9 \times 10^3} = 2.0019$$

$$e_D = \frac{\ln \frac{2.0019 \times 10^{-4}}{10^{-9}}}{\ln 10^{10}} = 5.3014.$$

Third approximation is

$$I_D = \frac{5 - \left[\frac{2.409}{15} + 1 \right] 5.3014}{21.9 \times 10^3}$$

$$= 2.0021$$

$$e_D = \frac{\ln \frac{2.0021 \times 10^{-4}}{10^9}}{\ln 10^{10}}$$

$$= 5.3014.$$

The calculations for I_D in stage 1 at the 9.276-V breakpoint are as follows:

First approximation is

$$I_D = \frac{V_2 - V_1 - \left[\frac{V_1}{V_3} + 1 \right] e_D}{R_1}$$

$$= \frac{9.276 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.5}{21.9 \times 10^3}$$

$$= 2.8706$$

$$e_D = \frac{\ln \frac{2.8706 \times 10^{-4}}{10^{-9}}}{\ln 10^{10}}$$

$$e_D = 0.54579.$$

Second approximation is

$$I_D = \frac{9.276 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.54523}{21.9 \times 10^3}$$

$$= 2.84636 \times 10^{-4}$$

$$e_D = \frac{\ln \frac{2.84636 \times 10^{-4}}{10^9}}{\ln 10^{10}}$$

$$= 0.545429.$$

Third approximation is

$$I_D = \frac{9.276 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.54159}{21.9 \times 10^3}$$

$$= 2.84673 \times 10^{-4}$$

$$e_D = 0.545432.$$

The calculations for I_D in stage 1 at the 10.3-V breakpoint are as follows:

First approximation is

$$I_D = \frac{V_2 - V_1 - \left[\frac{V_1}{V_3} + 1 \right] e_D}{R_1}$$

$$= \frac{10.3 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.5}{21.9 \times 10^3}$$

$$= 3.07324 \times 10^{-4}$$

$$e_D = \frac{\ln \frac{3.07324 \times 10^{-4}}{10^{-9}}}{\ln 10^{10}}$$

$$= 0.548759676.$$

Second approximation is

$$I_D = \frac{10.3 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.54876}{21.5}$$

$$= 3.31237 \times 10^{-4}$$

$$e_D = \frac{\ln \frac{3.31237 \times 10^{-4}}{10^{-9}}}{\ln 10^{10}}$$

$$= 0.5520140.$$

Third approximation is

$$I_D = \frac{10.3 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.5520140}{21.9 \times 10^9}$$

$$= 3.310654 \times 10^{-4}$$

$$e_D = \frac{\ln 3.310654 \times 10^{-4} \times 10^9}{10^{10}}$$

$$= 0.55199138.$$

Fourth approximation is

$$I_D = \frac{10.3 - 2.409 - \left[\frac{2.409}{15} + 1 \right] 0.55199178}{21.9 \times 10^3}$$

$$= 3.310666 \times 10^{-4}$$

$$e_D = \frac{\ln 3.310666 \times 10^{-4} \times 10^9}{\ln 10^{10}}$$

$$= 0.5519915.$$

The calculations for the other stages are accomplished in the same manner and are as listed in Table B-1.

APPENDIX C

TEST EQUIPMENT

VOLT METERS/VOM

Digital Volt Meter

Minimum requirements:

Range: 0 to 20 V

Resolution: 1% of Full Scale

Acceptable Instrument: Data Precision; model 24J or equivalent

Analog Volt-Ohm Meters (2 each)

Minimum requirements:

AC-DC Voltage Range: 0 to 300 V in 8 ranges, each range attenuation = 10 dB

Resistance Range: 0 to 1 M Ω

Meter Calibrated in dB.

Acceptable Instrument: Heath-Schlumberger; model SUR 666 or equivalent

SIGNAL SOURCES

Audio Oscillators (2 each)

Minimum requirements:

Sine Wave Output

Range: 1 Hz to 10 kHz

Voltage Range: 0 to 2 V peak to peak

Acceptable Instrument: HP model 200 AB or equivalent

AM Modulator (Special Design)

Figure C-1 is a schematic of a circuit which can easily be constructed and will serve as the test signal source when configured as shown in figure C-2.

Pulse Generator

Minimum Requirements:

Pulse Amplitude: -20 V maximum

Polarity: positive or negative

Pulse Width: -15 ns – 40 ms

Rep. Rate: 0-10 KC

Acceptable Instrument: Hewlett-Packard; model 1917A or equivalent

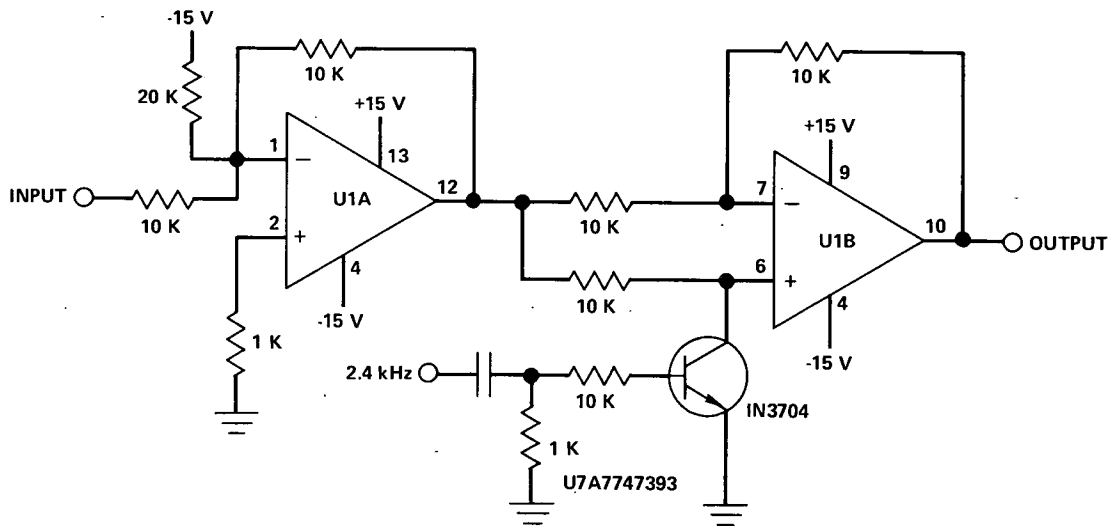


Figure C-1. Test Signal Source Schematic

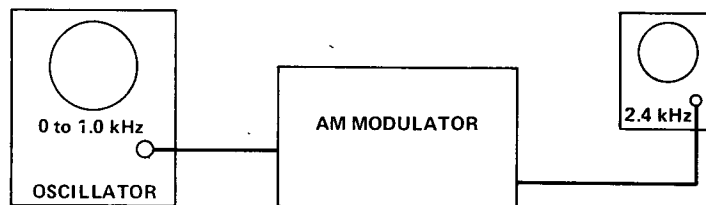


Figure C-2. Test Signal Source Configuration

OSCILLOSCOPE

Minimum Requirements

Bandwidth: dc to 500 kHz, two channel displays
 Vertical amplifier
 Sweep mode
 Sweep frequency by internal or external signals
 Bandwidth: dc to 50 kHz
 Acceptable Instrument: Tektronix; model 221

DIGITAL COUNTER

Minimum Requirements:

Range: 0 to 10 kHz
 Acceptable Instrument: Hewlett-Packard; model 5245L or equivalent

APPENDIX D

CIRCUIT DESCRIPTION

The logic used in the scan converter is "positive logic" and therefore logic "1's" are represented by positive voltage levels and logic "0's" are represented by 0 voltage levels. The integrated circuit types most often found in the scan converter are NAND, AND, OR, NOR, D type flip-flops, a.c. coupled flip-flops, summing operational amplifiers and integrating operational amplifiers. The following is a description of each of these circuits.

NAND GATE



TRUTH TABLE

V_{in_1}	V_{in_2}	V_{out_1}
0	0	1
0	1	1
1	0	1
1	1	0

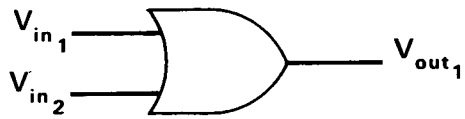
AND GATE



TRUTH TABLE

V_{in_1}	V_{in_2}	V_{out_1}
0	0	0
0	1	0
1	0	0
1	1	1

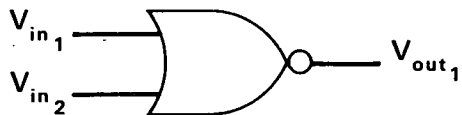
OR GATE



TRUTH TABLE

V_{in_1}	V_{in_2}	V_{out_1}
0	0	0
0	1	1
1	0	1
1	1	1

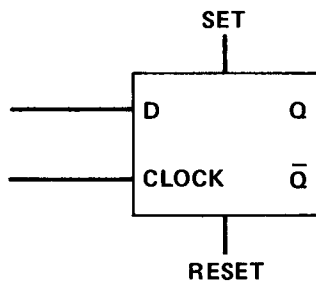
NOR GATE



TRUTH TABLE

V_{in_1}	V_{in_2}	V_{out_1}
0	0	1
0	1	0
1	0	0
1	1	0

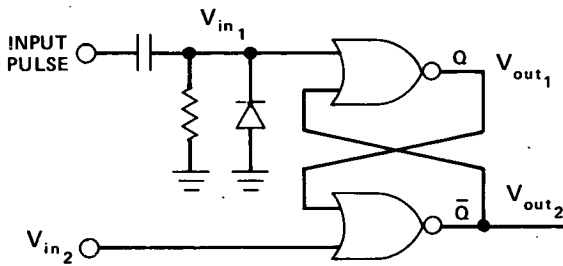
D-Type Flip-Flop



TRUTH TABLE

Set	Reset	t_n	t_{n+1}	
		D	Q	\bar{Q}
0	0	0	0	1
0	0	1	1	0

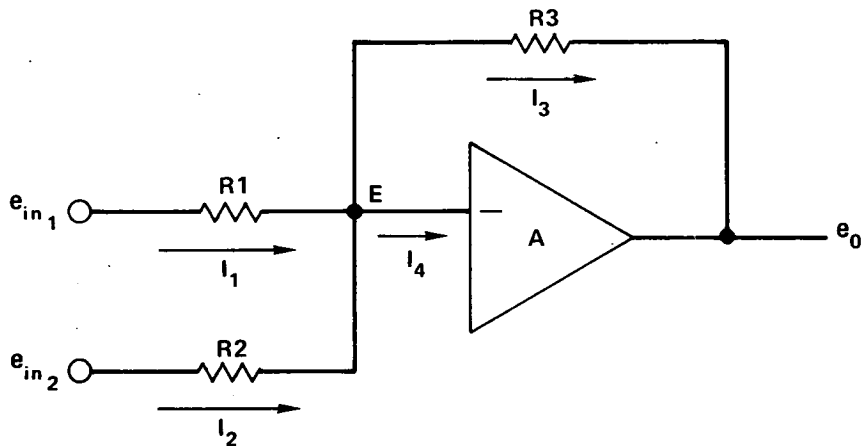
AC Coupled Flip-Flop



TRUTH TABLE

t_n		t_{n+1}	
V_{in_1}	V_{in_2}	Q	\bar{Q}
0	0	0	1
0	1	1	0
1	0	Not allowed	
1	1	Not allowed	

SUMMING OPERATIONAL AMPLIFIER



$$I_1 = \frac{e_{in_1} - E}{R_1} = \frac{e_{in_1}}{R_1} - \frac{E}{R_1}$$

$$I_2 = \frac{e_{in_2} - E}{R_2} = \frac{e_{in_2}}{R_2} - \frac{E}{R_2}$$

$$I_3 = I_1 + I_2 - I_4$$

$$\frac{e_{in_1}}{R_1} + \frac{e_{in_2}}{R_2} - \left[\frac{1}{R_1} + \frac{1}{R_2} \right] E - I_4 = I_3 \quad (1)$$

$$E = I_3 R_3 + e_0$$

$$I_3 = \frac{E}{R_3} - \frac{e_0}{R_3} \quad (2)$$

Substituting equation (2) into equation (1)

$$\begin{aligned} \frac{e_{in_1}}{R_1} + \frac{e_{in_2}}{R_2} - \left[\frac{1}{R_1} + \frac{1}{R_2} \right] E - I_4 &= \frac{E}{R_3} - \frac{e_0}{R_3} \\ -\frac{e_0}{R_3} &= \frac{e_{in_1}}{R_1} + \frac{e_{in_2}}{R_2} - \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right] E \end{aligned}$$

If R_A = internal resistance of the input to the amplifier,

then

$$E = I_4 R_A$$

$$I_4 = -\frac{e_0}{A}$$

$$E = -\frac{e_0}{A} R_A$$

$$-\frac{e_0}{R_3} = \frac{e_{in_1}}{R_1} + \frac{e_{in_2}}{R_2} - \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right] \frac{e_0}{A} R_A \quad (3)$$

and since

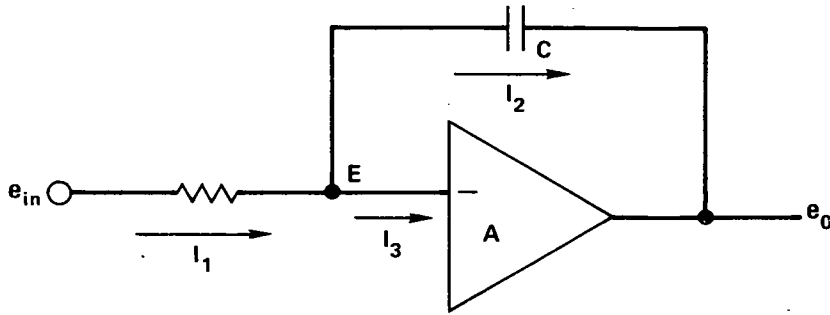
$$E = \frac{e_0}{A} R_A$$

and if the gain of the amplifier is very large, E approaches zero and equation (3) reduces to

$$\frac{e_0}{R_3} = \left[\frac{e_{in_1}}{R_1} + \frac{e_{in_2}}{R_2} \right]$$

which shows that the output of the amplifier e_0 is the sum of the input voltage e_{in_1} and e_{in_2} scaled by R_1 , R_2 , and R_3 .

INTEGRATOR OPERATIONAL AMPLIFIER



The voltage (V_C) across capacitor C is $V_C = \frac{q}{c}$ where q is the charge across the capacitor and c is the value of the capacitance in farads. By definition

$$\frac{dq}{dt} = I_2$$

$$dq = I_2 dt$$

$$q = \int I_2 dt$$

$$V_C = \frac{1}{C} \int I_2 dt$$

By inspection of the figure shown above

$$E = V_1 + e_o$$

$$I_2 = I_1 - I_3 \tag{1}$$

$$e_o = E - V_C$$

$$e_o = E - \frac{1}{C} \int I_2 dt \tag{2}$$

Further inspection shows

$$E = I_3 R_A$$

where R_A is the internal resistance of the amplifier

$$I_3 = \frac{E}{R_A}$$

and

$$e_0 = -I_3 A$$

so

$$I_3 = -\frac{e_0}{A}$$

Therefore,

$$E = -\frac{e_0 R_A}{A_2} \quad (3)$$

Substituting equation (1) and (3) into equation (2)

$$e_0 = \frac{e_0 R_A}{A}$$
$$-\frac{1}{C} \int (I_1 - I_3) dt = \frac{e_0 R_A}{A} - \frac{1}{C} \int \left(I_1 + \frac{e_0}{A} \right) dt \quad (4)$$

$$e_{in} = I_1 R_1 + E$$

$$I_1 = \frac{e_{in} - E}{R_1} = \frac{e_{in}}{R_1} - \frac{E}{R_1} \quad (5)$$

Substituting equation (5) into equation (4)

$$e_0 = \frac{e_0 R_A}{A} - \frac{1}{C} \int \left(\frac{e_{in}}{R_1} - \frac{E}{R_1} + \frac{e_0}{A} \right) dt \quad (6)$$

Substituting equation (3) into equation (6)

$$e_0 = \frac{e_0 R_A}{A} - \frac{1}{C} \int \left(\frac{e_{in}}{R_1} + \frac{e_0 R_A}{A R_1} + \frac{e_0}{A} \right) dt \quad (7)$$

If A is very large, equation (7) reduces to

$$e_0 = \frac{1}{C} \int \frac{e_{in}}{R} dt = -\frac{1}{RC} \int e_{in} dt$$

showing that the output voltage of the integrator operational amplifier is the inverse integral of the input voltage scaled by the resistor R and capacitor C .

APPENDIX E
APT DIGITAL SCAN CONVERTER PARTS LIST

Card 1

Symbol	Description	Part No.	Vendor
R14, 16, 18	Potentiometers, trimming, 50 K	6034	Amphenol
U1, 3, 8, 13, 14, 15	Timer/delays	NE555V	Signetics
U2, 4, 7, 12	NOR gates, quad input	CD4001AE	RCA
U5, 9	Counter, Binary, 14 stage, ripple	CD4020AE	RCA
U6	Dual D, flip-flop/set-reset	CD4013AE	RCA
U16	Counter, Binary, 12 stage, ripple	CD4040AE	RCA
U17	NAND gate	CD4048	RCA
U18	NAND gate	CD4012	RCA
Q1	Transistor, NPN, silicon	2N3565	—
—	Resistors, ¼ W, 5 percent	—	—
—	*Capacitors, µf, Mylar film, epoxy-encased pf, silvered mica	—	—

Card 2

Symbol	Description	Part No.	Vendor
U1 through U24	Shift Register, 1024-bit	2533V	Signetics
U25, 26, 27	AND/OR select gates, quad	CD4019AE	RCA

*Capacitors—All capacitors above 1000 pf. are to be Mylar film, epoxy-encased. Those below this value are silvered mica.

Card 3

Symbol	Description	Part No.	Vendor
R2, R6	Potentiometers, Linear, 10 K	3006W	Bourns
U1	Analog to Digital Converter, 8-bit	ZD460	Zeltex
U2	Digital to Analog Converter, 8-bit	DAC371-8	Hybrid System
U3	Amplifier, operational, single	U5B7741393	Fairchild
—	Resistors, ¼ W, 5 percent	—	—
—	*Capacitors, µf, Mylar film, epoxy-encased pf, silvered mica	—	—

Card 4

Symbol	Description	Part No.	Vendor
CR1, 2	Diodes, silicon	IN3604	—
Q1	Transistor, NPN, silicon	2N3704	—
R1 and R24	Potentiometers, Linear, 10 K	3006W	Bourns
R39	Potentiometer, Linear, 1 K	3006W	Bourns
U1 through U4	Amplifiers, operational, dual	U7A7747393	Fairchild
—	Resistors, ¼ W, 5 percent	—	—
—	*Capacitors, µf, Mylar film, epoxy-encased pf, silvered mica	—	—

Card 5

Symbol	Description	Part No.	Vendor
CR1 through CR8	Diodes, silicon	IN3604	—
CR9	Diode, zener, 6.8 V	LVA68A	—
Q2, 3, 4	Transistors, NPN, silicon	2N2219	—
U1 through U5	Amplifiers, operational, dual	U7A7747393	Fairchild
U6	Timer/delay	NE555V	Signetics
—	Resistors, ¼ W, 5 percent	—	—
—	*Capacitors, µf, Mylar film, epoxy-encased pf, silvered mica	—	—

*Capacitors—All capacitors above 1000 pf. are to be Mylar film, epoxy-encased. Those below this value are silvered mica.

Card 6

Symbol	Description	Part No.	Vendor
CR1 through CR8	Diodes, silicon	IN3604	—
Q1	Transistor, NPN, silicon	2N3702	—
R33	Potentiometer, Linear, 10 K	3006W	Bourns
U1 through U5	Amplifiers, operational, single	U5B7741393	Fairchild
U6, U7	Dual D, flip-flop/set-reset	CD4013AE	RCA
U8	NOR gate, quad input	CD4001AE	RCA
U9, 10, 11	Timer/delays	NE555V	Signetics
—	Resistors, ¼ W, 5 percent	—	—
—	*Capacitors, µf, Mylar film, epoxy-encased pf, silvered mica	—	—

Power Supplies/Precision Clock

Symbol	Description	Part No.	Vendor
—	Power supplies (2), standard, input 115/230 V at 47 to 440 Hz, 15 V at 0.7 amps	SP15-15	Standard Power, Inc.
—	Power supply, standard, input 115/230 V at 47 to 440 Hz, 5 V at 1.5 amps	SP15-5	Standard Power, Inc.
—	Precision Clock, 2.4 kHz	9ELEFS32	American Time Clock

*Capacitors—All capacitors above 1000 pf. are to be Mylar film, epoxy-encased. Those below this value are silvered mica.

Front Panel

Symbol	Description	Part No.	Vendor
J101 through J110	Connectors, BNC, 50 ohms (Front and Rear Panels)	UG/U 31-221	Amphenol
R104	Potentiometer, 500 K, single turn	504UA	Allen-Bradley
R108	Potentiometer, 50 K, single turn	503UA	Allen-Bradley
R115	Potentiometer, 20 K, 10 turn, w/dial	3400	Bourns
R116	Potentiometer, 2 K, 10 turn, w/dial	3400	Bourns
S101	Power Switch, toggle, SPST	MST215N	ALCO
S102	NOR/LIN COR Switch, toggle, DPDT	MST215N	ALCO
S103	Switch, Rotary, 2-5 positions	T206	CTS
S104	VIS/IR Switch, toggle, SPDT	MST115D	ALCO



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